KS8995MA

Integrated 5-Port 10/100 Managed Switch

Rev 2.4

General Description

The KS8995MA is a highly integrated Layer 2 managed switch with optimized bill of materials (BOM) cost for low port count, cost-sensitive 10/100Mbps switch systems. It also provides an extensive feature set such as tag/port-based VLAN, quality of service (QoS) priority, management, MIB counters, dual MII interfaces and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

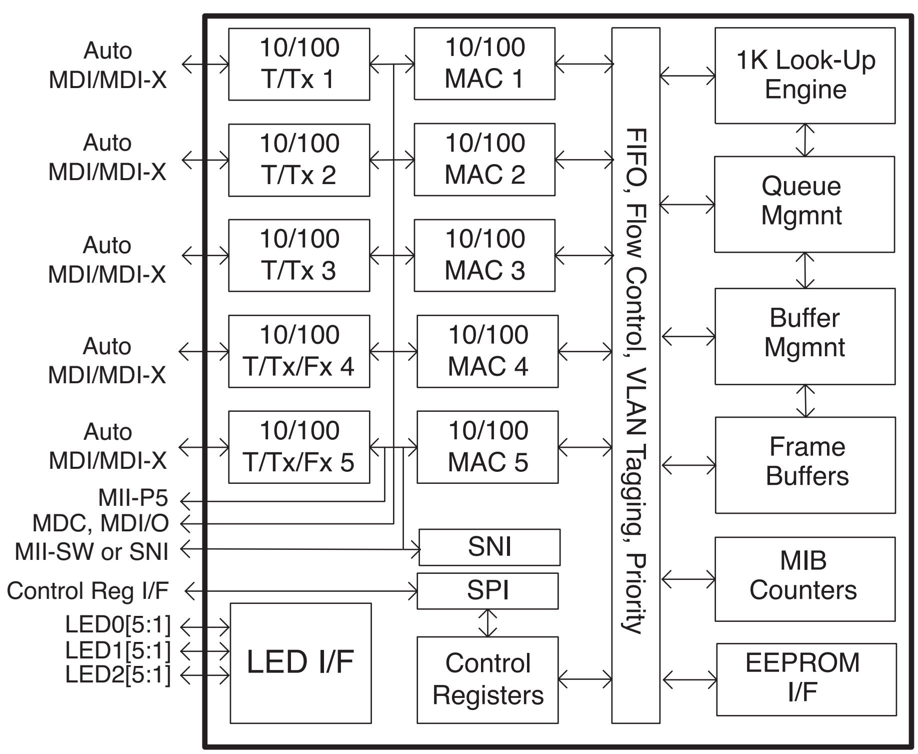
The KS8995MA contains five 10/100 transceivers with patented mixed-signal low-power technology, five media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

All PHY units support 10BASE-T and 100BASE-TX. In addition, two of the PHY units support 100BASE-FX (ports 4 and 5).

Features

- Integrated switch with five MACs and five Fast Ethernet transceivers fully compliant to IEEE 802.3u standard
- Shared memory based switch fabric with fully non-blocking configuration
- 1.4Gbps high-performance memory bandwidth
- 10BASE-T, 100BASE-TX, and 100BASE-FX modes (FX in ports 4 and 5)
- Dual MII configuration: MII-Switch (MAC or PHY mode MII) and MII-P5 (PHY mode MII)
- IEEE 802.1q tag-based VLAN (16 VLANs, full-range VID) for DMZ port, WAN/LAN separation or inter-VLAN switch links
- VLAN ID tag/untag options, per-port basis
- Programmable rate limiting 0Mbps to 100Mbps, ingress and egress port, rate options for high and low priority, per-port basis in 32Kbps increments
- Flow control or drop packet rate limiting (ingress port)
- Integrated MIB counters for fully compliant statistics gathering, 34 MIB counters per port

Functional Diagram



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Features (continued)

- Enable/Disable option for huge frame size up to 1916 bytes per frame
- IGMP v1/v2 snooping for multicast packet filtering
- Special tagging mode to send CPU info on ingress packet's port value
- SPI slave (complete) and MDIO (MII PHY only) serial management interface for control of register configuration
- MAC-id based security lock option
- Control registers configurable on-the-fly (port-priority, 802.1p/d/q, AN...)
- CPU read access to MAC forwarding table entries
- 802.1d Spanning Tree Protocol
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
- Broadcast storm protection with % control – global and per-port basis
- Optimization for fiber-to-copper media conversion
- Full-chip hardware power-down support (register configuration not saved)
- Per-port based software power-save on PHY (idle link detection, register configuration preserved)
- QoS/CoS packets prioritization supports: per port, 802.1p and DiffServ based
- 802.1p/q tag insertion or removal on a per-port basis (egress)
- MDC and MDI/O interface support to access the MII PHY control registers (not all control registers)
- MII local loopback support
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table)
- Wire-speed reception and transmission
- Integrated look-up engine with dedicated 1K MAC addresses
- Full duplex IEEE 802.3x and half-duplex back pressure flow control
- Comprehensive LED support
- 7-wire SNI support for legacy MAC interface
- Automatic MDI/MDI-X crossover for plug-and-play
- Disable automatic MDI/MDI-X option
- Low power:
  - Core: 1.8V
  - I/O: 2.5V or 3.3V
- 0.18μm CMOS technology
- Commercial temperature range: 0°C to +70°C
- Industrial temperature range: –40°C to +85°C
- Available in 128-pin PQFP package

Applications

- Broadband gateway/firewall/VPN
- Integrated DSL or cable modem multi-port router
- Wireless LAN access point plus gateway
- Home networking expansion
- Standalone 10/100 switch
- Hotel/campus/MxU gateway
- Enterprise VoIP gateway/phone
- FTTx customer premise equipment
- Managed Media converter

Ordering Information

Part Number	Temp. Range	Package	Lead Finish
KS8995MA	0°C to +70°C	128-Pin PQFP	Standard
KSZ8995MA	0°C to +70°C	128-Pin PQFP	Lead-Free
KS8995MAI	–40°C to +85°C	128-Pin PQFP	Standard

Revision History

Revision	Date	Summary of Changes
2.0	10/10/03	Created.
2.1	10/30/03	Editorial changes on electrical characteristics.
2.2	4/1/04	Editorial changes on the TTL input and output electrical characteristics.
2.3	1/19/05	Insert recommended reset circuit., Pg. 70. Editorial, Pg. 36
2.4	4/13/05	Changed VDDIO to 3.3V. Changed Jitter to 16 ns Max.

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System Level Applications

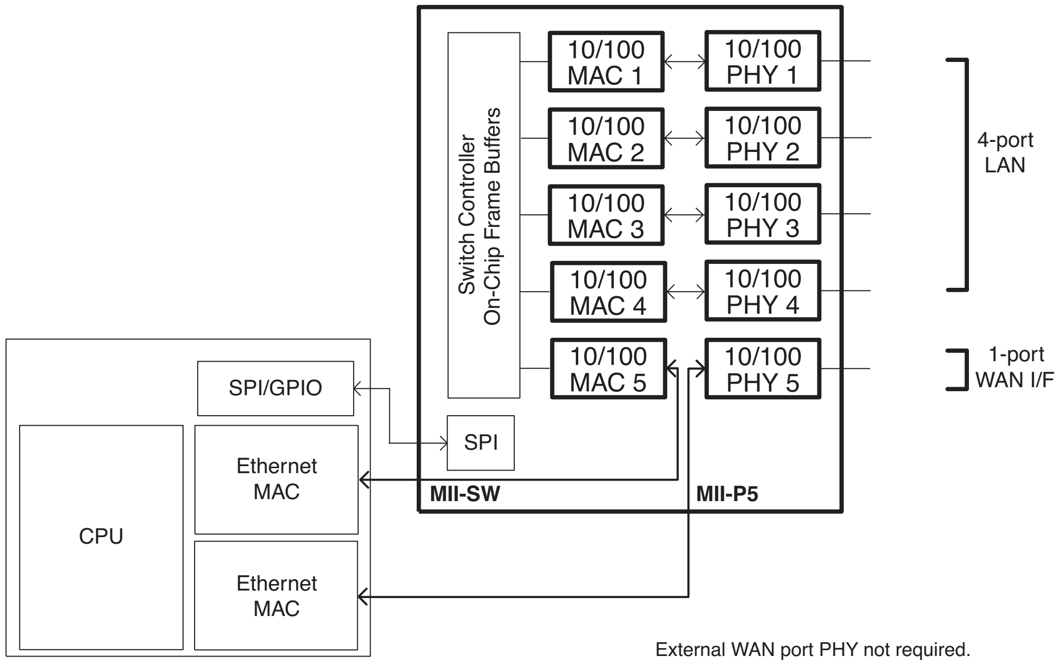


Figure 1. Broadband Gateway

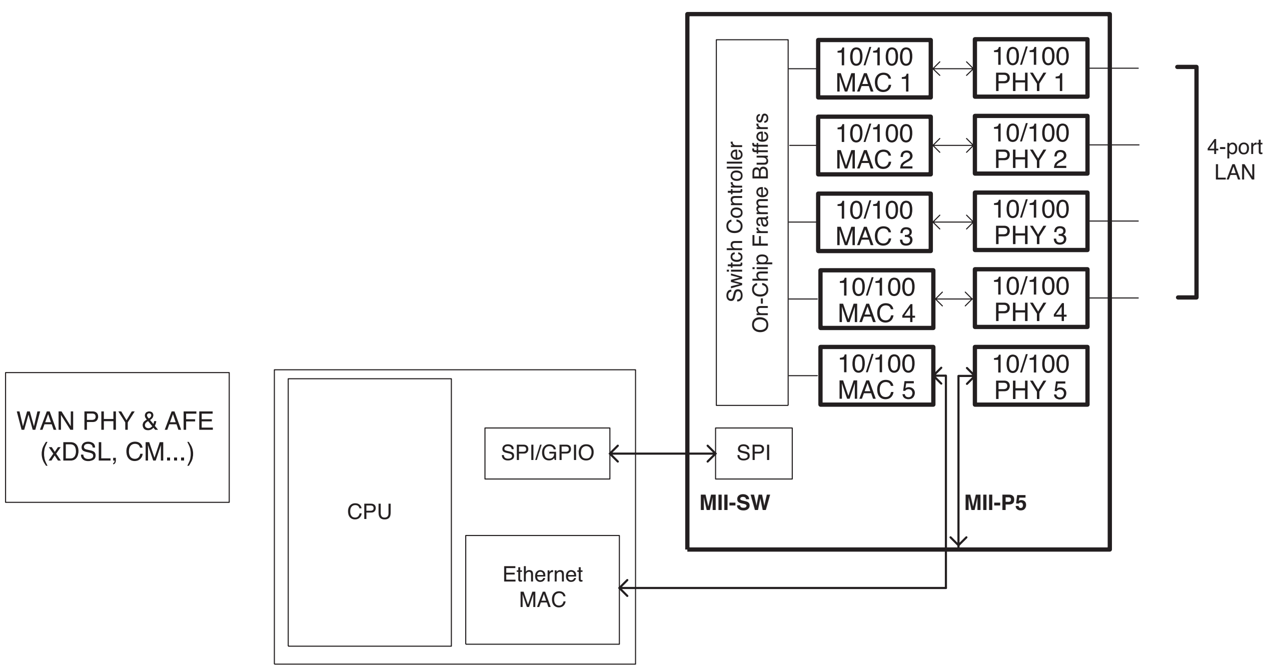


Figure 2. Integrated Broadband Router

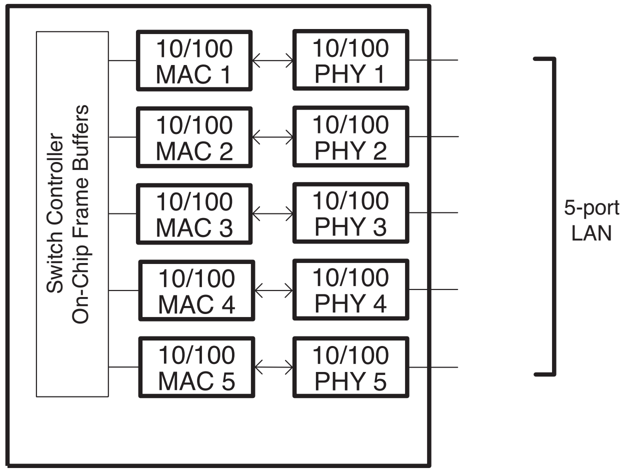


Figure 3. Standalone Switch

Pin Description (by Number)

Pin Number	Pin Name	Type[(1)]	Port	Pin Function[(2)]
1	MDI-XDIS	Ipd	1-5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GNDA	Gnd		Analog ground.
3	VDDAR	P		1.8V analog V_{DD}.
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal – (differential).
6	GNDA	Gnd		Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal – (differential).
9	VDDAT	P		2.5V or 3.3V analog V_{DD}.
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal - (differential).
12	GNDA	Gnd		Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
15	VDDAR	P		1.8V analog V_{DD}.
16	GNDA	Gnd		Analog ground.
17	ISET			Set physical transmit output current. Pull-down with a 3.01kΩ 1% resistor.
18	VDDAT	P		2.5V or 3.3V analog V_{DD}.
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal – (differential).
21	GNDA	Gnd		Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
24	VDDAT	P		2.5V or 3.3V analog V_{DD}.
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal – (differential).
27	GNDA	Gnd		Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
30	GNDA	Gnd		Analog ground.

Note:

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   Gnd = Ground.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pin pull-down.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[(1)]</th><th>Port</th><th colspan="3">Pin Function</th></tr>
<tr><td>31</td><td>VDDAR</td><td>P</td><td></td><td colspan="3">1.8V analog V_{DD}.</td></tr>
<tr><td>32</td><td>RXP5</td><td>I</td><td>5</td><td colspan="3">Physical receive signal + (differential).</td></tr>
<tr><td>33</td><td>RXM5</td><td>I</td><td>5</td><td colspan="3">Physical receive signal – (differential).</td></tr>
<tr><td>34</td><td>GNDA</td><td>Gnd</td><td></td><td colspan="3">Analog ground.</td></tr>
<tr><td>35</td><td>TXP5</td><td>O</td><td>5</td><td colspan="3">Physical transmit signal + (differential).</td></tr>
<tr><td>36</td><td>TXM5</td><td>O</td><td>5</td><td colspan="3">Physical transmit signal – (differential).</td></tr>
<tr><td>37</td><td>VDDAT</td><td>P</td><td></td><td colspan="3">2.5V or 3.3V analog V_{DD}.</td></tr>
<tr><td>38</td><td>FXSD5</td><td>I</td><td>5</td><td colspan="3">Fiber signal detect/factory test pin.</td></tr>
<tr><td>39</td><td>FXSD4</td><td>I</td><td>4</td><td colspan="3">Fiber signal detect/factory test pin.</td></tr>
<tr><td>40</td><td>GNDA</td><td>Gnd</td><td></td><td colspan="3">Analog ground.</td></tr>
<tr><td>41</td><td>VDDAR</td><td>P</td><td></td><td colspan="3">1.8V analog V_{DD}.</td></tr>
<tr><td>42</td><td>GNDA</td><td>Gnd</td><td></td><td colspan="3">Analog ground.</td></tr>
<tr><td>43</td><td>VDDAR</td><td>P</td><td></td><td colspan="3">1.8V analog V_{DD}.</td></tr>
<tr><td>44</td><td>GNDA</td><td>Gnd</td><td></td><td colspan="3">Analog ground.</td></tr>
<tr><td>45</td><td>MUX1</td><td>NC</td><td></td><td colspan="3" rowspan="2">Factory test pins. MUX1 and MUX2 should be left unconnected for normal operation.</td></tr>
<tr><td rowspan="3">46</td><td rowspan="3">MUX2</td><td rowspan="3">NC</td><td rowspan="3"></td></tr>
<tr><td>Mode</td><td>MUX1</td><td>MUX2</td></tr>
<tr><td>Normal Operation</td><td>NC</td><td>NC</td></tr>
<tr><td>47</td><td>PWRDN_N</td><td>Ipu</td><td></td><td colspan="3">Full-chip power down. Active low.</td></tr>
<tr><td>48</td><td>RESERVE</td><td>NC</td><td></td><td colspan="3">Reserved pin. No connect.</td></tr>
<tr><td>49</td><td>GNDD</td><td>Gnd</td><td></td><td colspan="3">Digital ground.</td></tr>
<tr><td>50</td><td>VDDC</td><td>P</td><td></td><td colspan="3">1.8V digital core V_{DD}.</td></tr>
<tr><td>51</td><td>PMTXEN</td><td>Ipd</td><td>5</td><td colspan="3">PHY[5] MII transmit enable.</td></tr>
<tr><td>52</td><td>PMTXD3</td><td>Ipd</td><td>5</td><td colspan="3">PHY[5] MII transmit bit 3.</td></tr>
<tr><td>53</td><td>PMTXD2</td><td>Ipd</td><td>5</td><td colspan="3">PHY[5] MII transmit bit 2.</td></tr>
<tr><td>54</td><td>PMTXD1</td><td>Ipd</td><td>5</td><td colspan="3">PHY[5] MII transmit bit 1.</td></tr>
<tr><td>55</td><td>PMTXD0</td><td>Ipd</td><td>5</td><td colspan="3">PHY[5] MII transmit bit 0.</td></tr>
<tr><td>56</td><td>PMTXER</td><td>Ipd</td><td>5</td><td colspan="3">PHY[5] MII transmit error.</td></tr>
<tr><td>57</td><td>PMTXC</td><td>O</td><td>5</td><td colspan="3">PHY[5] MII transmit clock. PHY mode MII.</td></tr>
<tr><td>58</td><td>GNDD</td><td>Gnd</td><td></td><td colspan="3">Digital ground.</td></tr>
<tr><td>59</td><td>VDDIO</td><td>P</td><td></td><td colspan="3">3.3V digital V_{DD} for digital I/O circuitry.</td></tr>
<tr><td>60</td><td>PMRXC</td><td>O</td><td>5</td><td colspan="3">PHY[5] MII receive clock. PHY mode MII.</td></tr>
</table>

Note:

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   Gnd = Ground.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Number	Pin Name	Type(1)	Port	Pin Function(2)
61	PMRXDV	Ipd/O	5	PHY[5] MII receive data valid.
62	PMRXD3	Ipd/O	5	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
63	PMRXD2	Ipd/O	5	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
64	PMRXD1	Ipd/O	5	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
65	PMRXD0	Ipd/O	5	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
66	PMRXER	Ipd/O	5	PHY[5] MII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.
67	PCRS	Ipd/O	5	PHY[5] MII carrier sense/force duplex mode. See “Register 76” for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails.
68	PCOL	Ipd/O	5	PHY[5] MII collision detect/force flow control. See “Register 66” for port 4 only. PD (default) = no force flow control. normal operation. PU = force flow control.
69	SMTXEN	Ipd		Switch MII transmit enable.
70	SMTXD3	Ipd		Switch MII transmit bit 3.
71	SMTXD2	Ipd		Switch MII transmit bit 2.
72	SMTXD1	Ipd		Switch MII transmit bit 1.
73	SMTXD0	Ipd		Switch MII transmit bit 0.
74	SMTXER	Ipd		Switch MII transmit error.
75	SMTXC	I/O		Switch MII transmit clock. Input in MAC mode, output in PHY mode MII.
76	GNDD	Gnd		Digital ground.
77	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry
78	SMRXC	I/O		Switch MII receive clock. Input in MAC mode, output in PHY mode MII.
79	SMRXDV	Ipd/O		Switch MII receive data valid
80	SMRXD3	Ipd/O		Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = enable switch MII full-duplex flow control.
81	SMRXD2	Ipd/O		Switch MII receive bit 2. Strap option: PD (default) = switch MII in full duplex mode; PU = switch MII in half-duplex mode.

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   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.
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   PD = Strap pin pull-down.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Port</th><th>Pin Function(2)</th></tr>
<tr><td>82</td><td>SMRXD1</td><td>Ipd/O</td><td></td><td>Switch MII receive bit 1. Strap option: PD (default) = switch MII in 100Mbps mode; PU = switch MII in 10Mbps mode.</td></tr>
<tr><td>83</td><td>SMRXD0</td><td>Ipd/O</td><td></td><td>Switch MII receive bit 0. Strap option: LED mode
PD (default) = mode 0; PU = mode 1. See “Register 11.”
<table>
<tr><th></th><th>Mode 0</th><th>Mode 1</th></tr>
<tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/Act</td></tr>
<tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/Act</td></tr>
<tr><td>LEDX_0</td><td>Speed</td><td>Full duplex</td></tr>
</table></td></tr>
<tr><td>84</td><td>SCOL</td><td>Ipd/O</td><td></td><td>Switch MII collision detect.</td></tr>
<tr><td>85</td><td>SCRS</td><td>Ipd/O</td><td></td><td>Switch MII carrier sense.</td></tr>
<tr><td>86</td><td>SCONF1</td><td>Ipd</td><td></td><td>Dual MII configuration pin.
<table>
<tr><th>Pin (91, 86, 87):</th><th>Switch MII</th><th>PHY [5] MII</th></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable</td><td>Disable</td></tr>
<tr><td>101</td><td>PHY Mode MII</td><td>PHY Mode MII</td></tr>
<tr><td>110</td><td>MAC Mode MII</td><td>PHY Mode MII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>PHY Mode MII</td></tr>
</table></td></tr>
<tr><td>87</td><td>SCONF0</td><td>Ipd</td><td></td><td>Dual MII configuration pin.</td></tr>
<tr><td>88</td><td>GNDD</td><td>Gnd</td><td></td><td>Digital ground.</td></tr>
<tr><td>89</td><td>VDDC</td><td>P</td><td></td><td>1.8V digital core V_{DD}.</td></tr>
<tr><td>90</td><td>LED5-2</td><td>Ipu/O</td><td>5</td><td>LED indicator 2. Strap option: aging setup. See “Aging” section.
PU (default) = aging enable; PD = aging disable.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>Ipu/O</td><td>5</td><td>LED indicator 1. Strap option: PU (default) = enable PHY MII I/F.
PD: tristate all PHY MII output. See “Pin 86 SCONF1.”</td></tr>
<tr><td>92</td><td>LED5-0</td><td>Ipu/O</td><td>5</td><td>LED indicator 0</td></tr>
<tr><td>93</td><td>LED4-2</td><td>Ipu/O</td><td>4</td><td>LED indicator 2</td></tr>
<tr><td>94</td><td>LED4-1</td><td>Ipu/O</td><td>4</td><td>LED indicator 1</td></tr>
<tr><td>95</td><td>LED4-0</td><td>Ipu/O</td><td>4</td><td>LED indicator 0</td></tr>
<tr><td>96</td><td>LED3-2</td><td>Ipu/O</td><td>3</td><td>LED indicator 2</td></tr>
<tr><td>97</td><td>LED3-1</td><td>Ipu/O</td><td>3</td><td>LED indicator 1</td></tr>
</table>

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   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up. Otri = Output tristated.
   PD = Strap pin pull-down. Fulld = Full duplex.

Pin Number	Pin Name	Type(1)	Port	Pin Function	
98	LED3-0	Ipu/O	3	LED indicator 0.	
99	GNDD	Gnd		Digital ground.	
100	VDDIO	P		3.3V digital V_{DD} for digital I/O.	
101	LED2-2	Ipu/O	2	LED indicator 2.	
102	LED2-1	Ipu/O	2	LED indicator 1.	
103	LED2-0	Ipu/O	2	LED indicator 0.	
104	LED1-2	Ipu/O	1	LED indicator 2.	
105	LED1-1	Ipu/O	1	LED indicator 1.	
106	LED1-0	Ipu/O	1	LED indicator 0.	
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock.	
108	MDIO	I/O	All	Switch or PHY[5] MII management data I/O. Features internal pull down to define pin state when not driven.	
109	SPIQ	Otri	All	(1) SPI serial data output in SPI slave mode; (2) not used in I^2C master mode. See “Pin 113.”	
110	SPIC/SCL	I/O	All	(1) Input clock up to 5MHz in SPI slave mode; (2) output clock at 81kHz in I^2C master mode. See “Pin 113.”	
111	SPID/SDA	I/O	All	(1) Serial data input in SPI slave mode; (2) serial data input/output in I^2C master mode. See “Pin 113.”	
112	SPIS_N	Ipu	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KS8995MA is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer; (2) not used in I^2C master mode.	
113	PS1	Ipd		Serial bus configuration pin. For this case, if the EEPROM is not present, the KS8995MA will start itself with the PS[1:0] **=** 00 default register values .	
				Pin Configuration	**Serial Bus Configuration**
				PS[1:0]=00	I^2C Master Mode for EEPROM
				PS[1:0]=01	Reserved
				PS[1:0]=10	SPI Slave Mode for CPU Interface
				PS[1:0]=11	Factory Test Mode (BIST)
114	PS0	Ipd		Serial bus configuration pin. See “Pin 113.”	
115	RST_N	Ipu		Reset the KS8995MA. Active low.	
116	GNDD	Gnd		Digital ground.	
117	VDDC	P		1.8V digital core V_{DD}.	
118	TESTEN	Ipd		NC for normal operation. Factory test pin.	

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   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Number	Pin Name	Type[1]	Port	Pin Function
119	SCANEN	Ipd		NC for normal operation. Factory test pin.
120	NC	NC		No connect.
121	X1	I		25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±100ppm.
122	X2	O		25MHz crystal clock connection.
123	VDDAP	P		1.8V analog V_{DD} for PLL.
124	GNDA	Gnd		Analog ground.
125	VDDAR	P		1.8V analog $V_{DD.}$
126	GNDA	Gnd		Analog ground.
127	GNDA	Gnd		Analog ground.
128	TEST2	NC		NC for normal operation. Factory test pin.

Note:

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   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Description (by Name)

Pin Number	Pin Name	Type(1)	Port	Pin Function
39	FXSD4	I	4	Fiber signal detect/factory test pin.
38	FXSD5	I	5	Fiber signal detect/factory test pin.
124	GNDA	Gnd		Analog ground.
42	GNDA	Gnd		Analog ground.
44	GNDA	Gnd		Analog ground.
2	GNDA	Gnd		Analog ground.
16	GNDA	Gnd		Analog ground.
30	GNDA	Gnd		Analog ground.
6	GNDA	Gnd		Analog ground.
12	GNDA	Gnd		Analog ground.
21	GNDA	Gnd		Analog ground.
27	GNDA	Gnd		Analog ground.
34	GNDA	Gnd		Analog ground.
40	GNDA	Gnd		Analog ground.
120	NC	NC		No connect.
127	GNDA	Gnd		Analog ground.
126	GNDA	Gnd		Analog ground.
49	GNDD	Gnd		Digital ground.
88	GNDD	Gnd		Digital ground.
116	GNDD	Gnd		Digital ground.
58	GNDD	Gnd		Digital ground.
76	GNDD	Gnd		Digital ground.
99	GNDD	Gnd		Digital ground.
17	ISET			Set physical transmit output current. Pull-down with a 3.01kΩ 1% resistor.
106	LED1-0	Ipu/O	1	LED indicator 0.
105	LED1-1	Ipu/O	1	LED indicator 1.
104	LED1-2	Ipu/O	1	LED indicator 2.
103	LED2-0	Ipu/O	2	LED indicator 0.
102	LED2-1	Ipu/O	2	LED indicator 1.
101	LED2-2	Ipu/O	2	LED indicator 2.
98	LED3-0	Ipu/O	3	LED indicator 0.

Note:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[(1)]</th><th>Port</th><th colspan="3">Pin Function[(2)]</th></tr>
<tr><td>97</td><td>LED3-1</td><td>Ipu/O</td><td>3</td><td colspan="3">LED indicator 1.</td></tr>
<tr><td>96</td><td>LED3-2</td><td>Ipu/O</td><td>3</td><td colspan="3">LED indicator 2.</td></tr>
<tr><td>95</td><td>LED4-0</td><td>Ipu/O</td><td>4</td><td colspan="3">LED indicator 0.</td></tr>
<tr><td>94</td><td>LED4-1</td><td>Ipu/O</td><td>4</td><td colspan="3">LED indicator 1.</td></tr>
<tr><td>93</td><td>LED4-2</td><td>Ipu/O</td><td>4</td><td colspan="3">LED indicator 2.</td></tr>
<tr><td>92</td><td>LED5-0</td><td>Ipu/O</td><td>5</td><td colspan="3">LED indicator 0.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>Ipu/O</td><td>5</td><td colspan="3">LED indicator 1. Strap option: PU (default) = enable PHY MII I/F
PD: tristate all PHY MII output. See “Pin 86 SCONF1.”</td></tr>
<tr><td>90</td><td>LED5-2</td><td>Ipu/O</td><td>5</td><td colspan="3">LED indicator 2. Strap option: aging setup. See “Aging” section.
(default) = aging enable; PD = aging disable.</td></tr>
<tr><td>107</td><td>MDC</td><td>Ipu</td><td>All</td><td colspan="3">Switch or PHY[5] MII management data clock.</td></tr>
<tr><td>108</td><td>MDIO</td><td>I/O</td><td>All</td><td colspan="3">Switch or PHY[5] MII management data I/O.</td></tr>
<tr><td>1</td><td>MDI-XDIS</td><td>Ipd</td><td>1-5</td><td colspan="3">Disable auto MDI/MDI-X.</td></tr>
<tr><td>45</td><td>MUX1</td><td>NC</td><td></td><td colspan="3" rowspan="2">Factory test pins. MUX1 and MUX2 should be left unconnected for normal operation.</td></tr>
<tr><td rowspan="3">46</td><td rowspan="3">MUX2</td><td rowspan="3">NC</td><td rowspan="3"></td></tr>
<tr><td>Mode</td><td>MUX1</td><td>MUX2</td></tr>
<tr><td>Normal Operation</td><td>NC</td><td>NC</td></tr>
<tr><td>68</td><td>PCOL</td><td>Ipd/O</td><td>5</td><td colspan="3">PHY[5] MII collision detect/force flow control. See “Register 18.”
For port 4 only. PD (default) = no force flow control. PU = force flow control.</td></tr>
<tr><td>67</td><td>PCRS</td><td>Ipd/O</td><td>5</td><td colspan="3">PHY[5] MII carrier sense/force duplex mode. See “Register 28.”
For port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails.</td></tr>
<tr><td>60</td><td>PMRXC</td><td>O</td><td>5</td><td colspan="3">PHY[5] MII receive clock. PHY mode MII.</td></tr>
<tr><td>65</td><td>PMRXD0</td><td>Ipd/O</td><td>5</td><td colspan="3">PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.</td></tr>
<tr><td>64</td><td>PMRXD1</td><td>Ipd/O</td><td>5</td><td colspan="3">PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.</td></tr>
<tr><td>63</td><td>PMRXD2</td><td>Ipd/O</td><td>5</td><td colspan="3">PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.</td></tr>
<tr><td>62</td><td>PMRXD3</td><td>Ipd/O</td><td>5</td><td colspan="3">PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.</td></tr>
<tr><td>61</td><td>PMRXDV</td><td>Ipd/O</td><td>5</td><td colspan="3">PHY[5] MII receive data valid.</td></tr>
<tr><td>66</td><td>PMRXER</td><td>Ipd/O</td><td>5</td><td colspan="3">PHY[5] MII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.</td></tr>
</table>

Note:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pin pull-down.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Port</th><th colspan="2">Pin Function</th></tr>
<tr><td>57</td><td>PMTXC</td><td>O</td><td>5</td><td colspan="2">PHY[5] MII transmit clock. PHY mode MII.</td></tr>
<tr><td>55</td><td>PMTXD0</td><td>Ipd</td><td>5</td><td colspan="2">PHY[5] MII transmit bit 0.</td></tr>
<tr><td>54</td><td>PMTXD1</td><td>Ipd</td><td>5</td><td colspan="2">PHY[5] MII transmit bit 1.</td></tr>
<tr><td>53</td><td>PMTXD2</td><td>Ipd</td><td>5</td><td colspan="2">PHY[5] MII transmit bit 2.</td></tr>
<tr><td>52</td><td>PMTXD3</td><td>Ipd</td><td>5</td><td colspan="2">PHY[5] MII transmit bit 3.</td></tr>
<tr><td>51</td><td>PMTXEN</td><td>Ipd</td><td>5</td><td colspan="2">PHY[5] MII transmit enable.</td></tr>
<tr><td>56</td><td>PMTXER</td><td>Ipd</td><td>5</td><td colspan="2">PHY[5] MII transmit error.</td></tr>
<tr><td>114</td><td>PS0</td><td>Ipd</td><td></td><td colspan="2">Serial bus configuration pin. See “Pin 113.”</td></tr>
<tr><td rowspan="6">113</td><td rowspan="6">PS1</td><td rowspan="6">Ipd</td><td rowspan="6"></td><td colspan="2">Serial bus configuration pin.
If EEPROM is not present, the KS8995MA will start itself with chip default (00)...</td></tr>
<tr><td>Pin Configuration</td><td>Serial Bus Configuration</td></tr>
<tr><td>PS[1:0]=00</td><td>I^{2}C Master Mode for EEPROM</td></tr>
<tr><td>PS[1:0]=01</td><td>Reserved</td></tr>
<tr><td>PS[1:0]=10</td><td>SPI Slave Mode for CPU Interface</td></tr>
<tr><td>PS[1:0]=11</td><td>Factory Test Mode (BIST)</td></tr>
<tr><td>47</td><td>PWRDN_N</td><td>Ipu</td><td></td><td colspan="2">Full-chip power down. Active low.</td></tr>
<tr><td>48</td><td>RESERVE</td><td>NC</td><td></td><td colspan="2">Reserved pin. No connect.</td></tr>
<tr><td>115</td><td>RST_N</td><td>Ipu</td><td></td><td colspan="2">Reset the KS8995MA. Active low.</td></tr>
<tr><td>5</td><td>RXM1</td><td>I</td><td>1</td><td colspan="2">Physical receive signal – (differential).</td></tr>
<tr><td>11</td><td>RXM2</td><td>I</td><td>2</td><td colspan="2">Physical receive signal – (differential).</td></tr>
<tr><td>20</td><td>RXM3</td><td>I</td><td>3</td><td colspan="2">Physical receive signal – (differential).</td></tr>
<tr><td>26</td><td>RXM4</td><td>I</td><td>4</td><td colspan="2">Physical receive signal – (differential).</td></tr>
<tr><td>33</td><td>RXM5</td><td>I</td><td>5</td><td colspan="2">Physical receive signal – (differential).</td></tr>
<tr><td>4</td><td>RXP1</td><td>I</td><td>1</td><td colspan="2">Physical receive signal + (differential).</td></tr>
<tr><td>10</td><td>RXP2</td><td>I</td><td>2</td><td colspan="2">Physical receive signal + (differential).</td></tr>
<tr><td>19</td><td>RXP3</td><td>I</td><td>3</td><td colspan="2">Physical receive signal + (differential).</td></tr>
<tr><td>25</td><td>RXP4</td><td>I</td><td>4</td><td colspan="2">Physical receive signal + (differential).</td></tr>
<tr><td>32</td><td>RXP5</td><td>I</td><td>5</td><td colspan="2">Physical receive signal + (differential).</td></tr>
<tr><td>119</td><td>SCANEN</td><td>Ipd</td><td></td><td colspan="2">NC for normal operation. Factory test pin.</td></tr>
<tr><td>84</td><td>SCOL</td><td>Ipd/O</td><td></td><td colspan="2">Switch MII collision detect.</td></tr>
<tr><td>87</td><td>SCONF0</td><td>Ipd</td><td></td><td colspan="2">Dual MII configuration pin.</td></tr>
</table>

Note:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   NC = No connect.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Port</th><th colspan="3">Pin Function[2]</th></tr>
<tr><td rowspan="10">86</td><td rowspan="10">SCONF1</td><td rowspan="10">Ipd</td><td rowspan="10"></td><td colspan="3">Dual MII configuration pin.</td></tr>
<tr><td>Pin (91, 86, 87):</td><td>Switch MII</td><td>PHY [5] MII</td></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable</td><td>Disable</td></tr>
<tr><td>101</td><td>PHY Mode MII</td><td>PHY Mode MII</td></tr>
<tr><td>110</td><td>MAC Mode MII</td><td>PHY Mode MII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>PHY Mode MII</td></tr>
<tr><td>85</td><td>SCRS</td><td>Ipd/O</td><td></td><td colspan="3">Switch MII carrier sense.</td></tr>
<tr><td>78</td><td>SMRXC</td><td>I/O</td><td></td><td colspan="3">Switch MII receive clock. Input in MAC mode, output in PHY mode MII.</td></tr>
<tr><td rowspan="5">83</td><td rowspan="5">SMRXD0</td><td rowspan="5">Ipd/O</td><td rowspan="5"></td><td colspan="3">Switch MII receive bit 0; strap option: LED mode
PD (default) = mode 0; PU = mode 1. See “Register 11.”</td></tr>
<tr><td></td><td>Mode 0</td><td>Mode 1</td></tr>
<tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/Act</td></tr>
<tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/Act</td></tr>
<tr><td>LEDX_0</td><td>Speed</td><td>Full duplex</td></tr>
<tr><td>82</td><td>SMRXD1</td><td>Ipd/O</td><td></td><td colspan="3">Switch MII receive bit 1. Strap option: PD (default) = switch MII in 100Mbps mode; PU = switch MII in 10Mbps mode.</td></tr>
<tr><td>81</td><td>SMRXD2</td><td>Ipd/O</td><td></td><td colspan="3">Switch MII receive bit 2. Strap option: PD (default) = switch MII in full-duplex mode; PU = switch MII in half-duplex mode.</td></tr>
<tr><td>80</td><td>SMRXD3</td><td>Ipd/O</td><td></td><td colspan="3">Switch MII receive bit 3. Strap option: PD (default) = disable switch MII full-duplex flow control; PU = enable switch MII full-duplex flow control.</td></tr>
<tr><td>79</td><td>SMRXDV</td><td>Ipd/O</td><td></td><td colspan="3">Switch MII receive data valid.</td></tr>
<tr><td>75</td><td>SMTXC</td><td>I/O</td><td></td><td colspan="3">Switch MII transmit clock. Input in MAC mode, output in PHY mode MII.</td></tr>
<tr><td>73</td><td>SMTXD0</td><td>Ipd</td><td></td><td colspan="3">Switch MII transmit bit 0.</td></tr>
<tr><td>72</td><td>SMTXD1</td><td>Ipd</td><td></td><td colspan="3">Switch MII transmit bit 1.</td></tr>
<tr><td>71</td><td>SMTXD2</td><td>Ipd</td><td></td><td colspan="3">Switch MII transmit bit 2.</td></tr>
<tr><td>70</td><td>SMTXD3</td><td>Ipd</td><td></td><td colspan="3">Switch MII transmit bit 3.</td></tr>
<tr><td>69</td><td>SMTXEN</td><td>Ipd</td><td></td><td colspan="3">Switch MII transmit enable.</td></tr>
<tr><td>74</td><td>SMTXER</td><td>Ipd</td><td></td><td colspan="3">Switch MII transmit error.</td></tr>
</table>

Note:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   Otri = Output tristated.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pin pull-down.
   Fulld = Full duplex.

Pin Number	Pin Name	Type(1)	Port	Pin Function
110	SPIC/SCL	I/O	All	(1) Input clock up to 5MHz in SPI slave mode; (2) Output clock at 81kHz in I^2C master mode. See "Pin 113."
111	SPID/SDA	I/O	All	(1) Serial data input in SPI slave mode; (2) Serial data input/output in I^2C master mode. See "Pin 113."
109	SPIQ	Otri	All	(1) SPI serial data output in SPI slave mode; (2) Not used in I^2C master mode. See "Pin 113."
112	SPIS_N	Ipu	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KS8995MA is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer; (2) Not used in I^2C master mode.
128	TEST2	NC		No connect for normal operation. Factory test pin.
118	TESTEN	Ipd		No connect for normal operation. Factory test pin.
8	TXM1	O	1	Physical transmit signal – (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
36	TXM5	O	5	Physical transmit signal – (differential).
7	TXP1	O	1	Physical transmit signal + (differential).
13	TXP2	O	2	Physical transmit signal + (differential).
22	TXP3	O	3	Physical transmit signal + (differential).
28	TXP4	O	4	Physical transmit signal + (differential).
35	TXP5	O	5	Physical transmit signal + (differential).
123	VDDAP	P		1.8V analog V_{DD} for PLL.
41	VDDAR	P		1.8V analog V_{DD}.
43	VDDAR	P		1.8V analog V_{DD}.
3	VDDAR	P		1.8V analog V_{DD}.
15	VDDAR	P		1.8V analog V_{DD}.
31	VDDAR	P		1.8V analog V_{DD}.
125	VDDAR	P		1.8V analog V_{DD}.
18	VDDAT	P		2.5V or 3.3V analog V_{DD}.
9	VDDAT	P		2.5V or 3.3V analog V_{DD}.
24	VDDAT	P		2.5V or 3.3V analog V_{DD}.
37	VDDAT	P		2.5V or 3.3V analog V_{DD}.
50	VDDC	P		1.8V digital core V_{DD}.

Note:

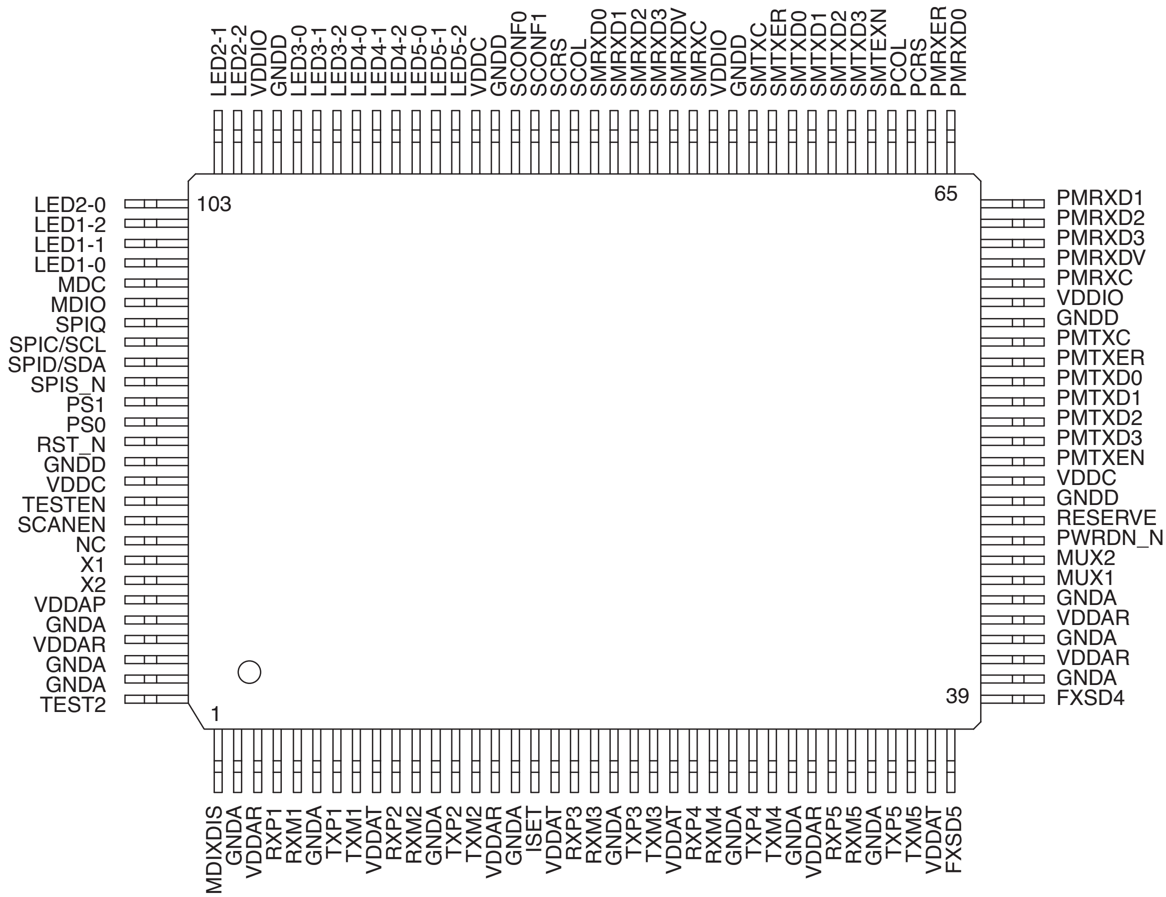
1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   Otri = Output tristated.
   NC = No connect.

Pin Number	Pin Name	Type[1]	Port	Pin Function
89	VDDC	P		1.8V digital core V_{DD}.
117	VDDC	P		1.8V digital core V_{DD}.
59	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
77	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
100	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
121	X1	I		25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±100ppm.
122	X2	O		25MHz crystal clock connection.

Note:

1. P = Power supply.
   I = Input.
   O = Output.

Pin Configuration



128-Pin PQFP (PQ)

Introduction

The KS8995MA contains five 10/100 physical layer transceivers and five media access control (MAC) units with an integrated Layer 2 managed switch. The device runs in three modes. The first mode is as a five-port integrated switch. The second is as a five-port switch with the fifth port decoupled from the physical port. In this mode, access to the fifth MAC is provided through a media independent interface (MII) . This is useful for implementing an integrated broadband router. The third mode uses the dual MII feature to recover the use of the fifth PHY. This allows the additional broadband gateway configuration, where the fifth PHY may be accessed through the MII-P5 port.

The KS8995MA has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the KS8995MA via the SPI bus, or partial control via the MDC/MDIO interface. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KS8995MA supports IEEE 802.3 10BASE-T, 100BASE-TX on all ports, and 100BASE-FX on ports 4 and 5. The KS8995MA can be used as two separate media converters.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

The major enhancements from the KS8995E to the KS8995MA are support for host processor management, a dual MII interface, tag as well as port based VLAN, spanning tree protocol support, IGMP snooping support, port mirroring support and rate limiting functionality.

Functional Overview: Physical Layer Transceiver

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KS8995MA generates 125MHz, 42MHz, 25MHz, and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator.

Scrambler/De-scrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

100BASE-FX Operation

100BASE-FX operation is very similar to 100BASE-TX operation except that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode the auto-negotiation feature is bypassed since there is no standard that supports fiber auto-negotiation.

100BASE-FX Signal Detection

The physical port runs in 100BASE-FX mode if FXSDx >0.6V for ports 4 and 5 only. This signal is internally referenced to 1.25V. The fiber module interface should be set by a voltage divider such that FXSDx ‘H’ is above this 1.25V reference, indicating signal

detect, and FXSDx 'L' is below the 1.25V reference to indicate no signal. When FXSDx is below 0.6V then 100BASE-FX mode is disabled. Since there is no auto-negotiation for 100BASE-FX mode, ports 4 and 5 must be forced to either full or half-duplex. Note that strap-in options exist to set duplex mode for port 4, but not for port 5.

100BASE-FX Far End Fault

Far end fault occurs when the signal detection is logically false from the receive fiber module. When this occurs, the transmission side signals the other end of the link by sending 84 1s followed by a zero in the idle period between frames. The far end fault may be disabled through register settings.

10BASE-T Transmit

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulsewidths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8995MA decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

Power Management

The KS8995MA features a per port power down mode. To save power the user can power down ports that are not in use by setting port control registers or MII control registers. In addition, it also supports full chip power down mode. When activated, the entire chip will be shutdown.

MDI/MDI-X Auto Crossover

The KS8995MA supports MDI/MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the Micrel device. This can be highly useful when end users are unaware of cable types and can also save on an additional uplink configuration connection. The auto crossover feature may be disabled through the port control registers.

Auto-Negotiation

The KS8995MA conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation the link partners advertise capabilities across the link to each other. If auto-negotiation is not supported or the link partner to the KS8995MA is forced to bypass auto-negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The flow for the link setup is shown in Figure 4.

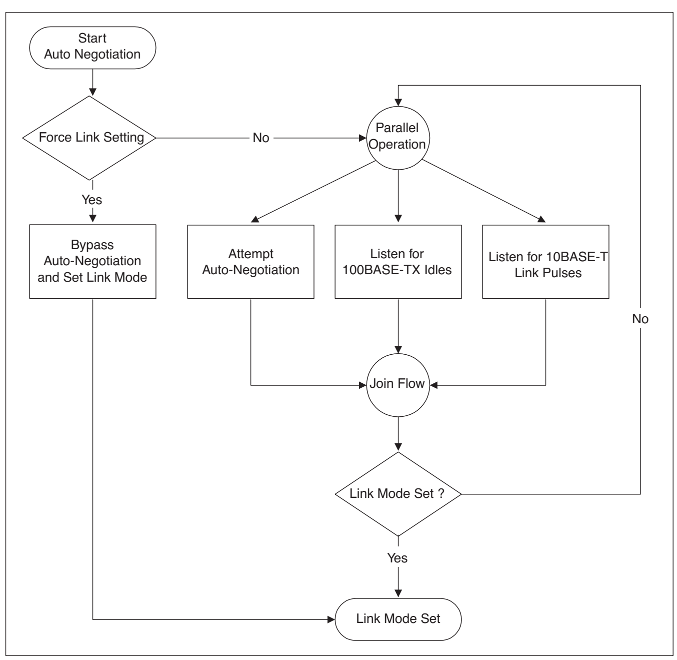


Figure 4. Auto-Negotiation

Functional Overview: Switch Core

Address Look-Up

The internal look-up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KS8995MA is guaranteed to learn 1K addresses and distinguishes itself from a hash-based look-up table, which depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal look-up engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted first to make room for the new entry.

Migration

The internal look-up engine also monitors whether a station is moved. If this occurs, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

Aging

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 + 75 seconds. This feature can be enabled or disabled through Register 3 or by external pull-up or pull-down resistors on LED[5][2]. See "Register 3" section.

Forwarding

The KS8995MA will forward packets using an algorithm that is depicted in the following flowcharts. Figure 5 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with "port to forward 1" (PTF1). PTF1 is then further modified by the spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with "port to forward 2" (PTF2), as shown in Figure 6. This is where the packet will be sent.

KS8995MA will not forward the following packets:

- Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
- 802.3x pause frames. The KS8995MA will intercept these packets and perform the appropriate actions.
- "Local" packets. Based on destination address (DA) look-up. If the destination port from the look-up table matches the port where the packet was from, the packet is defined as "local".

Switching Engine

The KS8995MA features a high-performance switching engine to move data to and from the MAC's, packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KS8995MA has a 64kB internal frame buffer. This resource is shared between all five ports. The buffer sharing mode can be programmed through Register 2. See "Register 2." In one mode, ports are allowed to use any free buffers in the buffer pool. In the second mode, each port is only allowed to use 1/5 of the total buffer pool. There are a total of 512 buffers available. Each buffer is sized at 128B.

Media Access Controller (MAC) Operation

The KS8995MA strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

Backoff Algorithm

The KS8995MA implements the IEEE Std 802.3 binary exponential back-off algorithm, and optional "aggressive mode" back off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration in Register 3. See "Register 3."

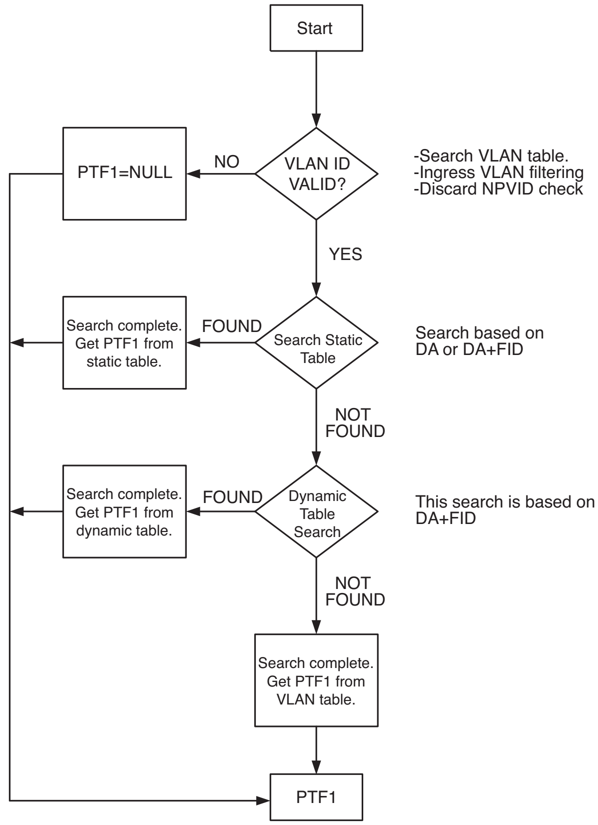


Figure 5. DA Look-Up Flowchart–Stage 1

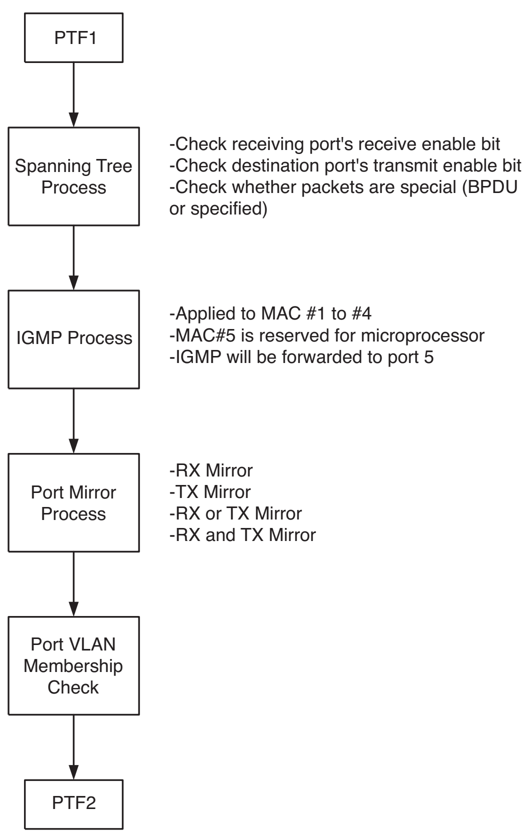


Figure 6. DA Resolution Flowchart–Stage 2

Late Collision

If a transmit packet experiences collisions after 512-bit times of the transmission, the packet is dropped.

Illegal Frames

The KS8995MA discards frames of less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Register 4. For special applications, the KS8995MA can also be programmed to accept frames up to 1916 bytes in Register 4. Since the KS8995MA supports VLAN tags, the maximum size is adjusted when these tags are present.

Flow Control

The KS8995MA supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KS8995MA receives a pause control frame, the KS8995MA will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value given in the second pause frame. During this period of flow control, only flow controlled packets from the KS8995MA are transmitted.

On the transmit side, the KS8995MA has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues, and available receive queues.

The KS8995MA flow controls a port that has just received a packet if the destination port resource is busy. The KS8995MA issues a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KS8995MA sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is also provided to prevent over-activation and deactivation of the flow control mechanism.

The KS8995MA flow controls all ports if the receive queue becomes full.

Half-Duplex Back Pressure

The KS8995MA also provides a half-duplex back pressure option (note: this is not in IEEE 802.3 standards). The activation and deactivation conditions are the same as the ones given for full-duplex mode. If back pressure is required, the KS8995MA sends preambles to defer the other station's transmission (carrier sense deference). To avoid jabber and excessive deference as defined in IEEE 802.3 standard, after a certain period of time, the KS8995MA discontinues carrier sense but raises it quickly after it drops packets to inhibit other transmissions. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in a carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier-sense-type back pressure is interrupted and those packets are transmitted instead. If there are no more packets to send, carrier-sense-type back pressure becomes active again until switch resources are free. If a collision occurs, the binary exponential backoff algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive backoff (Register 3, bit 0)
- No excessive collision drop (Register 4, bit 3)
- Back pressure (Register 4, bit 5)

These bits are not set as the default because this is not the IEEE standard.

Broadcast Storm Protection

The KS8995MA has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets are normally forwarded to all ports except the source port and thus use too many switch resources (bandwidth and available space in transmit queues). The KS8995MA has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally and can be enabled or disabled on a per port basis. The rate is based on a 50ms interval for 100BT and a 500ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Registers 6 and 7. The default setting for Registers 6 and 7 is 0x4A (74 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec ¥ 50ms/interval ¥ 1% = 74 frames/interval (approx.) = 0x4A

MII Interface Operation

The media independent interface (MII) is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. The KS8995MA provides two such interfaces. The MII-P5 interface is used to connect to the fifth PHY, whereas the MII-SW interface is used to connect to the fifth MAC. Each of these MII interfaces contains two distinct groups of signals, one for transmission and the other for receiving. Table 1 describes the signals used in the MII-P5 interface.

SNI Signal	Description	KS8995MA Signal
MTXEN	Transmit enable	PMTXEN
MTXER	Transmit error	PMTXER
MTXD3	Transmit data bit 3	PMTXD[3]
MTXD2	Transmit data bit 2	PMTXD[2]
MTXD1	Transmit data bit 1	PMTXD[1]
MTXD0	Transmit data bit 0	PMTXD[0]
MTXC	Transmit clock	PMTXC
MCOL	Collision detection	PCOL
MCRS	Carrier sense	PCRS
MRXDV	Receive data valid	PMRXDV
MRXER	Receive error	PMRXER
MRXD3	Receive data bit 3	PMRXD[3]
MRXD2	Receive data bit 2	PMRXD[2]
MRXD1	Receive data bit 1	PMRXD[1]
MRXD0	Receive data bit 0	PMRXD[0]
MRXC	Receive clock	PMRXC
MDC	Management data clock	MDC
MDIO	Management data I/O	MDIO

Table 1. MII – P5 Signals (PHY Mode)

PHY Mode Connection			MAC Mode Connection	
External MAC	KS8995MA Signal	Description	External PHY	KS8995MA Signal
MTXEN	SMTXEN	Transmit enable	MTXEN	SMRXDV
MTXER	SMTXER	Transmit error	MTXER	Not used
MTXD3	SMTXD[3]	Transmit data bit 3	MTXD3	SMRXD[3]
MTXD2	SMTXD[2]	Transmit data bit 2	MTXD2	SMRXD[2]
MTXD1	SMTXD[1]	Transmit data bit 1	MTXD1	SMRXD[1]
MTXD0	SMTXD[0]	Transmit data bit 0	MTXD0	SMRXD[0]
MTXC	SMTXC	Transmit clock	MTXC	SMRXC
MCOL	SCOL	Collision detection	MCOL	SCOL
MCRS	SCRS	Carrier sense	MCRS	SCRS
MRXDV	SMRXDV	Receive data valid	MRXDV	SMTXEN
MRXER	Not used	Receive error	MRXER	SMTXER
MRXD3	SMRXD[3]	Receive data bit 3	MRXD3	SMTXD[3]
MRXD2	SMRXD[2]	Receive data bit 2	MRXD2	SMTXD[2]
MRXD1	SMRXD[1]	Receive data bit 1	MRXD1	SMTXD[1]
MRXD0	SMRXD[0]	Receive data bit 0	MRXD0	SMTXD[0]
MRXC	SMRXC	Receive clock	MRXC	SMTXC

Table 2. MII – SW Signals

The MII-P5 interface operates in PHY mode only, while the MII-SW interface operates in either MAC mode or PHY mode. These interfaces are nibble-wide data interfaces and therefore run at 1/4 the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors. For half-duplex operation there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the MII-SW interface for PHY mode operation and the signal MTXER is not provided on the MII-SW interface for MAC mode operation. Normally MRXER would indicate a receive error coming from the physical layer device. MTXER would indicate a transmit error from the MAC device. These signals are not appropriate for this configuration. For PHY mode operation, if the device interfacing with the KS8995MA has an MRXER pin, it should be tied low. For MAC mode operation, if the device interfacing with the KS8995MA has an MTXER pin, it should be tied low.

SNI Interface Operation

The serial network interface (SNI) is compatible with some controllers used for network layer protocol processing. This interface can be directly connected to these types of devices. The signals are divided into two groups, one for transmission and the other for reception. The signals involved are described in Table 3.

SNI Signal	Description	KS8995MA Signal
TXEN	Transmit enable	SMTXEN
TXD	Serial transmit data	SMTXD[0]
TXC	Transmit clock	SMTXC
COL	Collision detection	SCOL
CRS	Carrier sense	SMRXDV
RXD	Serial receive data	SMRXD[0]
RXC	Receive clock	SMRXC

Table 3. SNI Signals

This interface is a bit-wide data interface and therefore runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Likewise, the receive side also has an indicator that shows if the data it is receiving is valid.

For half-duplex operation, there is a signal that indicates if a collision has occurred during transmission.

Advanced Functionality

Spanning Tree Support

Port 5 is the designated port for spanning tree support.

The other ports (port 1 – port 4) can be configured in one of the five spanning tree states via “transmit enable,” “receive enable,” and “learning disable” register settings in Registers 18, 34, 50, and 66 for ports 1, 2, 3, and 4, respectively. The following description shows the port setting and software actions taken for each of the five spanning tree states.

Disable state: the port should not forward or receive any packets. Learning is disabled.

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 1."

Software action: the processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with “overriding bit” set) and the processor should discard those packets. Note: processor is connected to port 5 via MII interface. Address learning is disabled on the port in this state.

Blocking state: only packets to the processor are forwarded. Learning is disabled.

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 1"

Software action: the processor should not send any packets to the port(s) in this state. The processor should program the “Static MAC table” with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.

Listening state: only packets to and from the processor are forwarded. Learning is disabled.

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 1."

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g. BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see “Special Tagging Mode” section for details. Address learning is disabled on the port in this state.

Learning state: only packets to and from the processor are forwarded. Learning is enabled.

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 0."

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see "Special Tagging Mode" section for details. Address learning is enabled on the port in this state.

Forwarding state: packets are forwarded and received normally. Learning is enabled.

Port setting: "transmit enable = 1, receive enable = 1, learning disable = 0."

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see "Special Tagging Mode" section for details. Address learning is enabled on the port in this state.

Special Tagging Mode

The special tagging mode is designed for spanning tree protocol IGMP snooping and is flexible for use in other applications. The special tagging mode, similar to 802.1q, requires software to change network drivers to insert/modify/strip/interpret the special tag. This mode is enabled by setting both Register 11 bit 0 and Register 80 bit 2.

802.1q Tag Format	Special Tag Format
TPID (tag protocol identifier, 0x8100) + TCI	STPID (special tag identifier, 0x8100) + TCI 0x810 + 4 bit for "port mask") + TCI

Table 4. Special Tagging Mode Format

The STPID will only be seen and used on the port 5 interface, which should be connected to a processor. Packets from the processor to the switch should be tagged with STPID and the port mask defined as below:

"0001" packet to port 1 only

"0010" packet to port 2 only

"0100" packet to port 3 only

"1000" packet to port 4 only

"0011" packet broadcast to port 1 and port 2.

.....

"1111" packet broadcast to port 1, 2, 3 and 4.

"0000" normal tag, will use the KS8995MA internal look-up result. Normal packets should use this setting. If packets from the processors do not have a tag, the KS8995MA will treat them as normal packets and an internal look-up will be performed.

The KS8995MA uses a non-zero "port mask" to bypass the look-up result and override any port setting, regardless of port states (blocking, disable, listening, learning). Table 5 shows the egress rules when dealing with STPID.

Ingress Tag Field	Tx Port "Tag Insertion"	Tx Port "Tag Removal"	Egress Action to Tag Field
(0x810+ port mask)	0	0	• Modify tag field to 0x8100. • Recalculate CRC. • No change to TCI if not null VID. • Replace VID with ingress (port 5) port VID if null VID.
(0x810+ port mask)	0	1	• (STPID + TCI) will be removed. • Padding to 64 bytes if necessary. • Recalculate CRC.
(0x810+ port mask)	1	0	• Modify tag field to 0x8100. • Recalculate CRC. • No change to TCI if not null VID. • Replace VID with ingress (port 5) port VID if null VID.
(0x810+ port mask)	1	1	• Modify tag field to 0x8100. • Recalculate CRC. • No change to TCI if not null VID. • Replace VID with ingress (port 5) port VID if null VID.
Not tagged	Don't care	Don't care	Determined by the dynamic MAC address table.

Table 5. STPID Egress Rules (Processor to Switch Port 5)

For packets from regular ports (port 1 - port 4) to port 5, the port mask is used to tell the processor which port the packet was received on, defined as:

"0001" from port 1,

"0010" from port 2,

"0100" from port 3,

"1000" from port 4

No values other than the previous four defined should be received in this direction in the special mode. Table 6 shows the egress rule for this direction.

Ingress Packets	Egress Action to Tag Field
Tagged with 0x8100 + TCI	• Modify TPID to 0x810 + "port mask," which indicates source port. • No change to TCI, if VID is not null. • Replace null VID with ingress port VID. • Recalculate CRC.
Not tagged	• Insert TPID to 0x810 + "port mask," which indicates source port. • Insert TCI with ingress port VID. • Recalculate CRC.

Table 6. STPID Egress Rules (Switch to Processor)

IGMP Support

There are two parts involved to support IGMP in Layer 2. The first part is "IGMP" snooping. The switch will trap IGMP packets and forward them only to the processor port. The IGMP packets are identified as IP packets (either Ethernet IP packets or IEEE 802.3 SNAP IP packets) AND IP version = 0x4 AND protocol number = 0x2. The second part is "multicast address insertion" in the static MAC table. Once the multicast address is programmed in the static MAC table, the multicast session will be trimmed to the subscribed ports, instead of broadcasting to all ports. To enable this feature, set Register 5 bit 6 to 1. Also "special tag mode" needs to be enabled, so that the processor knows which port the IGMP packet was received on. Enable "special tag mode" by setting both Register 11 bit 0 and Register 80 bit 2.

Port Mirroring Support

KS8995MA supports “port mirror” comprehensively as:

1. “Receive Only” mirror on a port. All the packets received on the port will be mirrored on the sniffer port. For example, port 1 is programmed to be “rx sniff,” and port 5 is programmed to be the “sniffer port.” A packet, received on port 1, is destined to port 4 after the internal look-up. The KS8995MA will forward the packet to both port 4 and port 5. KS8995MA can optionally forward even “bad” received packets to port 5.
2. “Transmit Only” mirror on a port. All the packets transmitted on the port will be mirrored on the sniffer port. For example, port 1 is programmed to be “tx sniff,” and port 5 is programmed to be the “sniffer port.” A packet, received on any of the ports, is destined to port 1 after the internal look-up. The KS8995MA will forward the packet to both ports 1 and 5.
3. “Receive and Transmit” mirror on two ports. All the packets received on port A AND transmitted on port B will be mirrored on the sniffer port. To turn on the “AND” feature, set Register 5 bit 0 to 1. For example, port 1 is programmed to be “rx sniff,” port 2 is programmed to be “transmit sniff,” and port 5 is programmed to be the “sniffer port.” A packet, received on port 1, is destined to port 4 after the internal look-up. The KS8995MA will forward the packet to port 4 only, since it does not meet the “AND” condition. A packet, received on port 1, is destined to port 2 after the internal look-up. The KS8995MA will forward the packet to both port 2 and port 5.

Multiple ports can be selected to be “rx sniffed” or “tx sniffed.” And any port can be selected to be the “sniffer port.” All these per port features can be selected through Register 17.

VLAN Support

KS8995MA supports 16 active VLANs out of 4096 possible VLANs specified in IEEE 802.1q. KS8995MA provides a 16-entry VLAN table, which converts VID (12 bits) to FID (4 bits) for address look-up. If a non-tagged or null-VID-tagged packet is received, the ingress port VID is used for look-up. In the VLAN mode, the look-up process starts with VLAN table look-up to determine whether the VID is valid. If the VID is not valid, the packet will be dropped and its address will not be learned. If the VID is valid, FID is retrieved for further look-up. FID+DA is used to determine the destination port. FID+SA is used for learning purposes.

DA found in Static MAC table	USE FID Flag?	FID Match?	DA+FID found in Dynamic MAC table	Action
No	Don’t care	Don’t care	No	Broadcast to the membership ports defined in the VLAN table bit [20:16].
No	Don’t care	Don’t care	Yes	Send to the destination port defined in the dynamic MAC table bit [54:52].
Yes	0	Don’t care	Don’t care	Send to the destination port(s) defined in the static MAC table bit [52:48].
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN table bit [20:16].
Yes	1	No	Yes	Send to the destination port defined in the dynamic MAC table bit [54:52].
Yes	1	Yes	Don’t care	Send to the destination port(s) defined in the static MAC table bit [52:48].

Table 7. FID+DA Look-Up in the VLAN Mode

SA+FID found in Dynamic MAC table	Action
No	The SA+FID will be learned into the dynamic table.
Yes	Time stamp will be updated.

Table 8. FID+SA Look-Up in the VLAN Mode

Advanced VLAN features are also supported in KS8995MA, such as “VLAN ingress filtering” and “discard non PVID” defined in Register 18 bit 6 and bit 5. These features can be controlled on a port basis.

Rate Limit Support

KS8995MA supports hardware rate limiting on “receive” and “transmit” independently on a per port basis. It also supports rate limiting in a priority or non-priority environment. The rate limit starts from 0Kbps and goes up to the line rate in steps of 32Kbps. The KS8995MA uses one second as an interval. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during this interval.

For receive, if the number of bytes exceeds the programmed limit, the switch will stop receiving packets on the port until the “one second” interval expires. There is an option provided for flow control to prevent packet loss. If the rate limit is programmed greater than or equal to 128Kbps and the byte counter is 8K bytes below the limit, the flow control will be triggered. If the rate limit is programmed lower than 128Kbps and the byte counter is 2K bytes below the limit, the flow control will be triggered.

For transmit, if the number of bytes exceeds the programmed limit, the switch will stop transmitting packets on the port until the “one second” interval expires.

If priority is enabled, the KS8995MA can support different rate controls for both high priority and low priority packets. This can be programmed through Registers 21–27.

Configuration Interface

The KS8995MA can function as a managed switch or unmanaged switch. If no EEPROM or micro-controller exists, the KS8995MA will operate from its default setting. Some default settings are configured via strap in options as indicated in the table below.

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>PU/PD[(1)]</th><th colspan="3">Description[(1)]</th></tr>
<tr><td>1</td><td>MDI-XDIS</td><td>Ipd</td><td colspan="3">Disable auto MDI/MDI-X.
PD = (default) = normal operation.
PU = disable auto MDI/MDI-X on all ports.</td></tr>
<tr><td>45</td><td>MUX1</td><td>NC</td><td colspan="3" rowspan="2">Factory test pins. MUX1 and MUX2 should be left unconnected for normal operation.</td></tr>
<tr><td rowspan="3">46</td><td rowspan="3">MUX2</td><td rowspan="3">NC</td></tr>
<tr><td>Mode</td><td>MUX1</td><td>MUX2</td></tr>
<tr><td>Normal Operation</td><td>NC</td><td>NC</td></tr>
<tr><td>62</td><td>PMRXD3</td><td>Ipd/O</td><td colspan="3">PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control;
PU = disable flow control.</td></tr>
<tr><td>63</td><td>PMRXD2</td><td>Ipd/O</td><td colspan="3">PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure;
PU = enable back pressure.</td></tr>
<tr><td>64</td><td>PMRXD1</td><td>Ipd/O</td><td colspan="3">PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.</td></tr>
<tr><td>65</td><td>PMRXD0</td><td>Ipd/O</td><td colspan="3">PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.</td></tr>
<tr><td>66</td><td>PMRXER</td><td>Ipd/O</td><td colspan="3">PHY[5] MII receive error. Strap option: PD (default) = 1522/1518 bytes;
PU = packet size up to 1536 bytes.</td></tr>
<tr><td>67</td><td>PCRS</td><td>Ipd/O</td><td colspan="3">PHY[5] MII carrier sense/force duplex mode. See “Register 76” for port 4 only.
PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails.</td></tr>
<tr><td>68</td><td>PCOL</td><td>Ipd/O</td><td colspan="3">PHY[5] MII collision detect/force flow control. See “Register 66” for port 4 only.
PD (default) = no force flow control. PU = force flow control.</td></tr>
<tr><td>80</td><td>SMRXD3</td><td>Ipd/O</td><td colspan="3">Switch MII receive bit 3. Strap option: PD (default) = disable switch MII full-duplex flow control; PU = enable switch MII full-duplex flow control.</td></tr>
<tr><td>81</td><td>SMRXD2</td><td>Ipd/O</td><td colspan="3">Switch MII receive bit 2. Strap option: PD (default) = switch MII in full-duplex mode;
PU = switch MII in half-duplex mode.</td></tr>
<tr><td>82</td><td>SMRXD1</td><td>Ipd/O</td><td colspan="3">Switch MII receive bit 1. Strap option: PD (default) = switch MII in 100Mbps mode;
PU = switch MII in 10Mbps mode.</td></tr>
<tr><td rowspan="5">83</td><td rowspan="5">SMRXD0</td><td rowspan="5">Ipd/O</td><td colspan="3">Switch MII receive bit 0; Strap option: LED mode PD (default) = mode 0;
PU = mode 1. See “Register 11.”</td></tr>
<tr><td></td><td>Mode 0</td><td>Mode 1</td></tr>
<tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/Act</td></tr>
<tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/Act</td></tr>
<tr><td>LEDX_0</td><td>Speed</td><td>Fulld</td></tr>
</table>

Note:

1. NC = No connect.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Fulld = Full duplex.

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>PU/PD[1]</th><th colspan="3">Description[1]</th></tr>
<tr><td rowspan="10">86</td><td rowspan="10">SCONF1</td><td rowspan="10">Ipd</td><td colspan="3">Dual MII configuration pin.</td></tr>
<tr><td>Pins 91, 86, 87</td><td>Switch MII</td><td>PHY [5] MII</td></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable</td><td>Disable</td></tr>
<tr><td>101</td><td>PHY Mode MII</td><td>PHY Mode MII</td></tr>
<tr><td>110</td><td>MAC Mode MII</td><td>PHY Mode MII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>PHY Mode MII</td></tr>
<tr><td>87</td><td>SCONF0</td><td>Ipd</td><td colspan="3">Dual MII configuration pin.</td></tr>
<tr><td>90</td><td>LED5-2</td><td>Ipu/O</td><td colspan="3">LED indicator 2. Strap option: Aging setup. See “Aging” section
PU (default) = aging enable; PD = aging disable.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>Ipu/O</td><td colspan="3">LED indicator 1. Strap option: PU (default): enable PHY MII I/F. PD: tristate all PHY MII output. See “Pin 86 SCONF1.”</td></tr>
<tr><td rowspan="6">113</td><td rowspan="6">PS1</td><td rowspan="6">Ipd</td><td colspan="3">Serial bus configuration pin.
For this case, if the EEPROM is not present, the KS8995MA will start itself with the PS[1:0] = 00 default register values .</td></tr>
<tr><td>Pin Configuration</td><td colspan="2">Serial Bus Configuration</td></tr>
<tr><td>PS[1:0]=00</td><td colspan="2">I²C Master Mode for EEPROM</td></tr>
<tr><td>PS[1:0]=01</td><td colspan="2">Reserved</td></tr>
<tr><td>PS[1:0]=10</td><td colspan="2">SPI Slave Mode for CPU Interface</td></tr>
<tr><td>PS[1:0]=11</td><td colspan="2">Factory Test Mode (BIST)</td></tr>
<tr><td>114</td><td>PS0</td><td>Ipd</td><td colspan="3">Serial bus configuration pin. See “Pin 113.”</td></tr>
<tr><td>128</td><td>TEST2</td><td>NC</td><td colspan="3">NC for normal operation. Factory test pin.</td></tr>
</table>

Note:

1. NC = No connect.
   Ipd = Input w/ internal pull-down.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   Otri = Output tristated.

I²C Master Serial Bus Configuration

If a 2-wire EEPROM exists, the KS8995MA can perform more advanced features like broadcast storm protection and rate control. The EEPROM should have the entire valid configuration data from Register 0 to Register 109 defined in the “Memory Map,” except the status registers. After reset, the KS8995MA will start to read all 110 registers sequentially from the EEPROM. The configuration access time (t_{prgm}) is less than 15ms as shown in Figure 7.

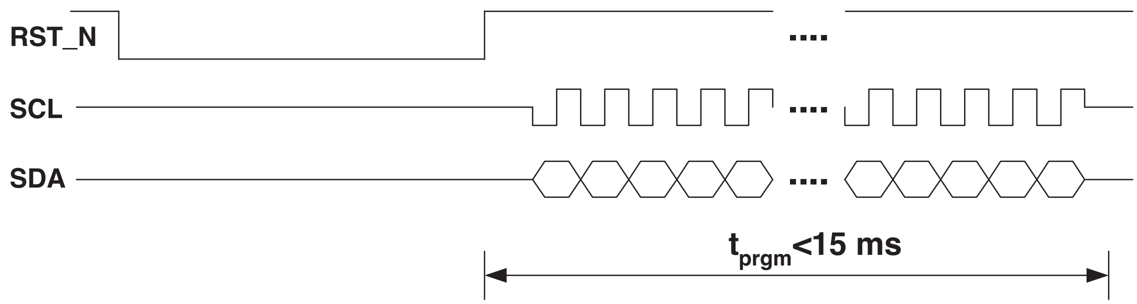


Figure 7. KS8995MA EEPROM Configuration Timing Diagram

To configure the KS8995MA with a pre-configured EEPROM use the following steps:

1. At the board level, connect pin 110 on the KS8995MA to the SCL pin on the EEPROM. Connect pin 111 on the KS8995MA to the SDA pin on the EEPROM.
2. Set the input signals PS[1:0] (pins 113 and 114, respectively) to “00.” This puts the KS8995MA serial bus configuration into I²C master mode.
3. Be sure the board-level reset signal is connected to the KS8995MA reset signal on pin 115 (RST_N).
4. Program the contents of the EEPROM before placing it on the board with the desired configuration data. Note that the first byte in the EEPROM must be “95” for the loading to occur properly. If this value is not correct, all other data will be ignored.
5. Place EEPROM on the board and power up the board. Assert the active-low board level reset to RST_N on the KS8995MA. After the reset is de-asserted, the KS8995MA will begin reading configuration data from the EEPROM. The configuration access time (t_{prgm}) is less than 15ms.

Note: For proper operation, make sure that pin 47 (PWRDN_N) is not asserted during the reset operation.

SPI Slave Serial Bus Configuration

The KS8995MA can also act as an SPI slave device. Through the SPI, the entire feature set can be enabled, including “VLAN,” “IGMP snooping,” “MIB counters,” etc. The external master device can access any register from Register 0 to Register 127 randomly. The system should configure all the desired settings before enabling the switch in the KS8995MA. To enable the switch, write a "1" to Register 1 bit 0.

Two standard SPI commands are supported (00000011 for “READ DATA,” and 00000010 for “WRITE DATA”). To speed configuration time, the KS8995MA also supports multiple reads or writes. After a byte is written to or read from the KS8995MA, the internal address counter automatically increments if the SPI Slave Select Signal (SPIS_N) continues to be driven low. If SPIS_N is kept low after the first byte is read, the next byte at the next address will be shifted out on SPIQ. If SPIS_N is kept low after the first byte is written, bits on the Master Out Slave Input (SPID) line will be written to the next address. Asserting SPIS_N high terminates a read or write operation. This means that the SPIS_N signal must be asserted high and then low again before issuing another command and address. The address counter wraps back to zero once it reaches the highest address. Therefore the entire register set can be written to or read from by issuing a single command and address.

The KS8995MA is able to support a 5MHz SPI bus. A high performance SPI master is recommended to prevent internal counter overflow.

To use the KS8995MA SPI:

1. At the board level, connect KS8995MA pins as follows:

KS8995MA Pin Number	KS8995MA Signal Name	Microprocessor Signal Description
112	SPIS_N	SPI Slave Select
110	SPIC	SPI Clock
111	SPID	Master Out Slave Input
109	SPIQ	Master In Slave Output

Table 9. SPI Connections

2. Set the input signals PS[1:0] (pins 113 and 114, respectively) to “10” to set the serial configuration to SPI slave mode.
3. Power up the board and assert a reset signal. After reset wait 100μs, the start switch bit in Register 1 will be set to ‘0’. Configure the desired settings in the KS8995MA before setting the start register to ‘1.'
4. Write configuration to registers using a typical SPI write data cycle as shown in Figure 8 or SPI multiple write as shown in Figure 10. Note that data input on SPID is registered on the rising edge of SPIC.
5. Registers can be read and configuration can be verified with a typical SPI read data cycle as shown in Figure 9 or a multiple read as shown in Figure 11. Note that read data is registered out of SPIQ on the falling edge of SPIC.
6. After configuration is written and verified, write a ‘1’ to Register 1 bit 0 to begin KS8995MA operation.

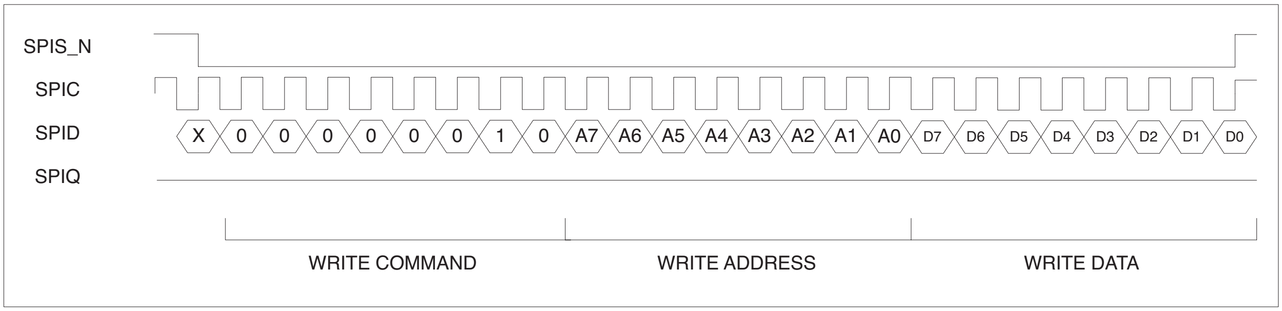


Figure 8. SPI Write Data Cycle

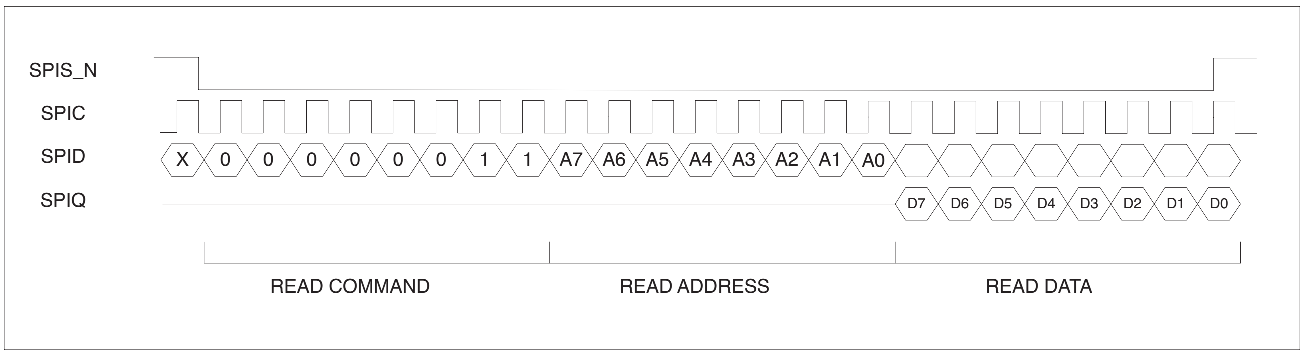


Figure 9. SPI Read Data Cycle

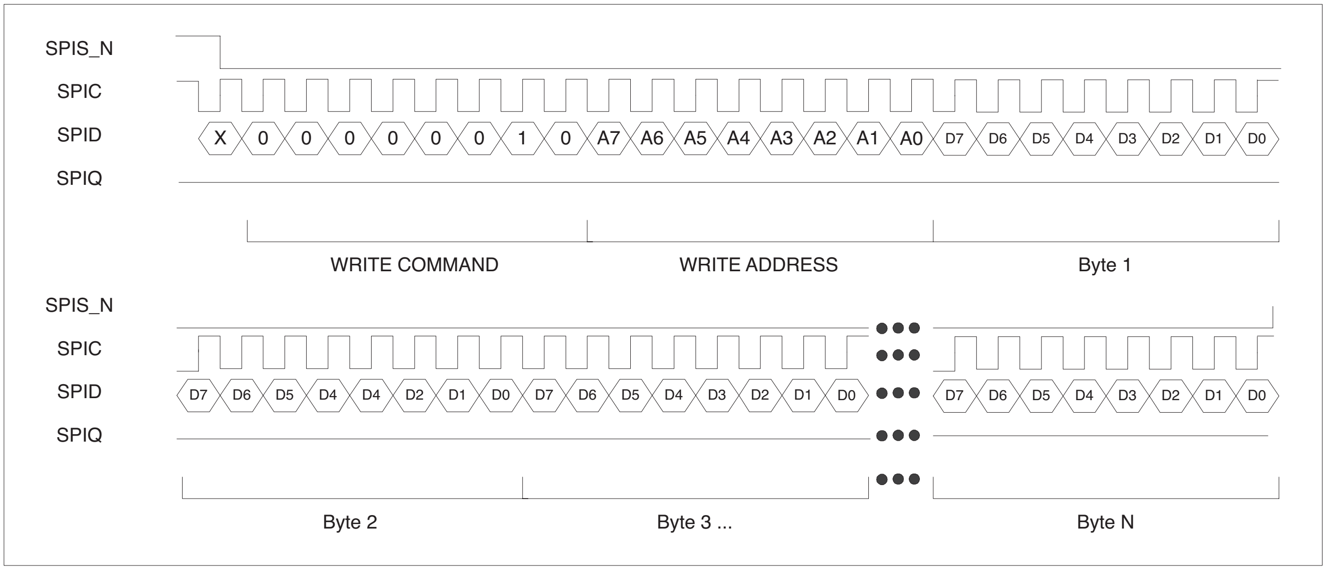


Figure 10. SPI Multiple Write

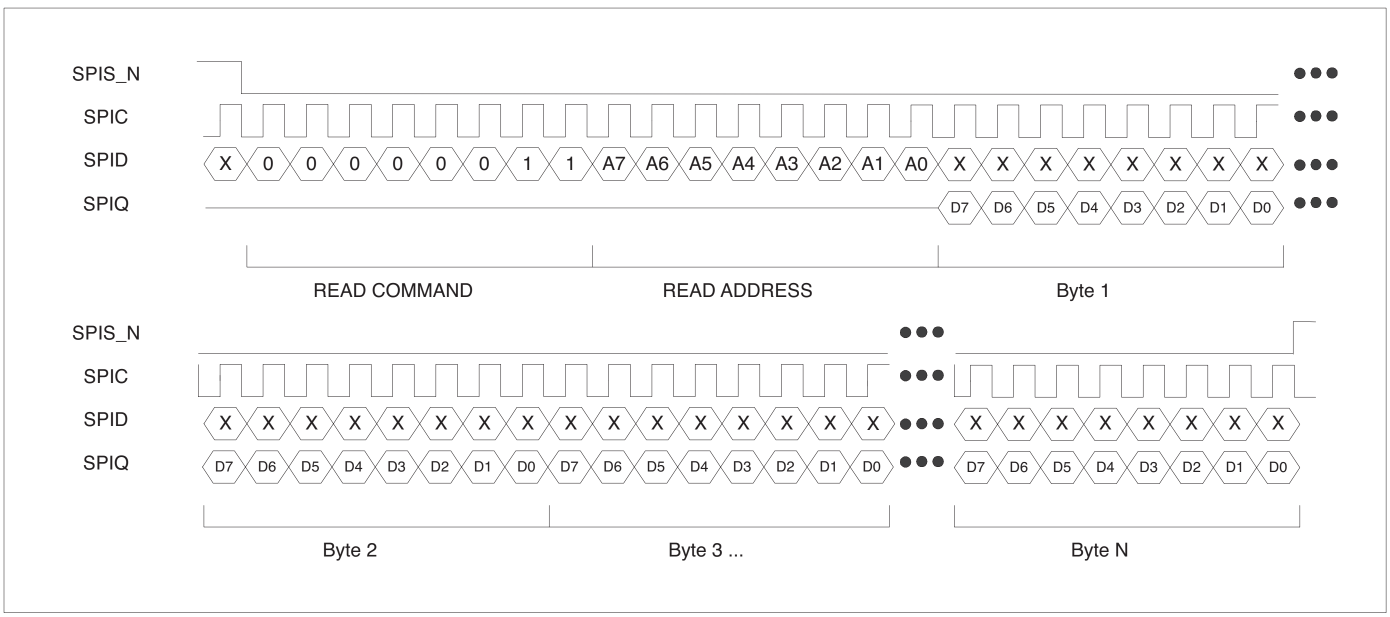


Figure 11. SPI Multiple Read

MII Management Interface (MIIM)

A standard MIIM interface is provided for all five PHY devices in the KS8995MA. An external device with MDC/MDIO capability is able to read PHY status or to configure PHY settings. For details on the MIIM interface standard please reference the IEEE 802.3 specification (section 22.2.4.5). The MIIM interface does not have access to all the configuration registers in the KS8995MA. It can only access the standard MII registers. See “MIIM Registers.” The SPI interface, on the other hand, can be used to access the entire KS8995MA feature set.

Register Description

Offset		
Decimal	**Hex**	**Description**
0-1	0x00-0x01	Chip ID Registers
2-11	0x02-0x0B	Global Control Registers
12-15	0x0C-0x0F	Reserved
16-29	0x10-0x1D	Port 1 Control Registers
30-31	0x1E-0x2F	Port 1 Status Registers
32-45	0x20-0x2D	Port 2 Control Registers
46-47	0x2E-0x2F	Port 2 Status Registers
48-61	0x30-0x3D	Port 3 Control Registers
62-63	0x3E-0x3F	Port 3 Status Registers
64-77	0x40-0x4D	Port 4 Control Registers
78-79	0x4E-0x4F	Port 4 Status Registers
80-93	0x50-0x5D	Port 5 Control Registers
94-95	0x5E-0x5F	Port 5 Status Registers
96-103	0x60-0x67	TOS Priority Control Registers
104-109	0x68-0x6D	MAC Address Registers
110-111	0x6E-0x6F	Indirect Access Control Registers
112-120	0x70-0x78	Indirect Data Registers
121-122	0x79-0x7A	Digital Testing Status Registers
123-124	0x7B-0x7C	Digital Testing Control Registers
125-126	0x7D-0x7E	Analog Testing Control Registers
127	0x7F	Analog Testing Status Register

Global Registers

Address	Name	Description	Mode	Default
Register 0 (0x00): Chip ID0				
7-0	Family ID	Chip family.	RO	0x95
Register 1 (0x01): Chip ID1 / Start Switch				
7-4	Chip ID	0x0 is assigned to M series. (95MA)	RO	0x0
3-1	Revision ID	Revision ID	RO	0x2
0	Start Switch	1, start the chip when external pins (PS1, PS0) = (1,0) or (0,1). Note: in (PS1,PS0) = (0,0) mode, the chip will start automatically, after trying to read the external EEPROM. If EEPROM does not exist, the chip will use default values for all internal registers. If EEPROM is present, the contents in the EEPROM will be checked. The switch will check: (1) Register 0 = 0x95, (2) Register 1 [7:4] = 0x0. If this check is OK, the contents in the EEPROM will override chip register default values =0, chip will not start when external pins (PS1, PS0) = (1,0) or (0,1). Note: (PS1, PS0) = (1,1) for factory test only.	RW	—

Address	Name	Description	Mode	Default
Register 2 (0x02): Global Control 0				
7	Reserved	Reserved.	R/W	0x0
6-4	802.1p Base Priority	Used to classify priority for incoming 802.1q packets "User priority" is compared against this value ⊕ : classified as high priority. < : classified as low priority.	R/W	0x4
3	Enable PHY MII	1, enable PHY MII interface. Note: if not enabled, the switch will tri-state all outputs.	R/W	Pin LED[5][1] strap option. Pull-down (0): isolate. Pull-up (1): Enable. Note: LED[5][1] has internal pull-up.
2	Buffer Share Mode	1, buffer pool is shared by all ports. A port can use more buffer when other ports are not busy. 0, a port is only allowed to use 1/5 of the buffer pool.	R/W	0x1
1	UNH Mode	1, the switch will drop packets with 0x8808 in T/L filed, or DA=01-80-C2-00-00-01. 0, the switch will drop packets qualified as "flow control" packets.	R/W	0
0	Link Change Age	1, link change from "link" to "no link" will cause fast aging (<800μs) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 + 75 seconds). Note: If any port is unplugged, all addresses will be automatically aged out.	R/W	0
Register 3 (0x03): Global Control 1				
7	Pass All Frames	1, switch all packets including bad ones. Used solely for debugging purpose. Works in conjunction with sniffer mode.	R/W	0
6	Reserved	Reserved.	R/W	0
5	IEEE 802.3x Transmit Flow Control Disable	0, will enable transmit flow control based on AN result. 1, will not enable transmit flow control regardless of AN result.	R/W	Pin PMRXD3 strap option. Pull-down(0): Enable Tx flow control. Pull-up(1): Disable Tx/Rx flow control. Note: PMRXD3 has internal pull-down.
4	IEEE 802.3x Receive Flow Control Disable	0, will enable receive flow control based on AN result. 1, will not enable receive flow control regardless of AN result. Note: Bit 5 and bit 4 default values are controlled by the same pin, but they can be programmed independently.	R/W	Pin PMRXD3 strap option. Pull-down (0): Enable Rx flow control. Pull-up (1): Disable Tx/Rx flow control. Note: PMRXD3 has internal pull-down.
3	Frame Length Field Check	1, will check frame length field in the IEEE packets If the actual length does not match, the packet will be dropped (for L/T <1500) .	R/W	0

Address	Name	Description	Mode	Default
2	Aging Enable	1, Enable age function in the chip. 0, Disable aging function.	R/W	Pin LED[5][2] strap option. Pull-down (0): Aging disable Pull-up (1): Aging enable. Note: LED[5][2] has internal pull up.
1	Fast age Enable	1 = Turn on fast age (800µs).	R/W	0
0	Aggressive Back Off Enable	1 = Enable more aggressive back-off algorithm in half duplex mode to enhance performance. This is not an IEEE standard.	R/W	Pin PMRXD0 strap option. Pull-down (0): Disable aggressive back off. Pull-up (1): Aggressive back off. Note: PMRXD0 has internal pull down.
Register 4 (0x04): Global Control 2				
7	Unicast Port-VLAN Mismatch Discard	This feature is used for port VLAN (described in Register 17, Register 33...). 1, all packets can not cross VLAN boundary. 0, unicast packets (excluding unknown/ multicast/broadcast) can cross VLAN boundary.	R/W	1
6	Multicast Storm Protection Disable	1, “Broadcast Storm Protection” does not include multicast packets. Only DA=FFFFFFFFFFFF packets will be regulated. 0, “Broadcast Storm Protection” includes DA = FFFFFFFFFFFF and DA[40] = 1 packets.	R/W	1
5	Back Pressure Mode	1, carrier sense based backpressure is selected. 0, collision based backpressure is selected.	R/W	1
4	Flow Control and Back Pressure Fair Mode	1, fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. 0, in this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be “fair” to the flow control port.	R/W	1
3	No Excessive Collision Drop	1, the switch will not drop packets when 16 or more collisions occur. 0, the switch will drop packets when 16 or more collisions occur.	R/W	Pin PMRXD1 strap option. Pull-down (0): Drop excessive collision packets. Pull-up (1): Don’t drop excessive collision packets. Note: PMRXD1 has internal pull down.
2	Huge Packet Support	1, will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of the same register. 0, the max packet size will be determined by bit 1 of this register.	R/W	0

Address	Name	Description	Mode	Default
1	Legal Maximum Packet Size Check Disable	1, will accept packet sizes up to 1536 bytes (inclusive). 0, 1522 bytes for tagged packets (not including packets with STPID from CPU to ports 1-4), 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.	R/W	Pin PMRXER strap option. Pull-down (0): 1518/1522 byte packets. Pull-up (1): 1536 byte packets. Note: PMRXER has internal pull-down.
0	Priority Buffer Reserve	1, each output queue is pre-allocated 48 buffers, used exclusively for high priority packets. It is recommended to enable this when priority queue feature is turned on. 0, no reserved buffers for high priority packets.	R/W	0
Register 5 (0x05): Global Control 3				
7	802.1q VLAN Enable	1, 802.1q VLAN mode is turned on. VLAN table needs to set up before the operation. 0, 802.1q VLAN is disabled.	R/W	0
6	IGMP Snoop Enable on Switch MII Interface	1, IGMP snoop enabled. All the IGMP packets will be forwarded to Switch MII port. 0, IGMP snoop disabled.	R/W	0
5	Enable Direct Mode on Switch MII Interface	1, direct mode on port 5. This is a special mode for the Switch MII interface. Using preamble before MRXDV to direct switch to forward packets, bypassing internal look-up. 0, normal operation.	R/W	0
4	Enable Pre-Tag on Switch MII Interface	1, packets forwarded to Switch MII interface will be pre-tagged with the source port number (preamble before MRXDV). 0, normal operation.	R/W	0
3-2	Priority Scheme Select	00 = always deliver high priority packets first. 01 = deliver high/low packets at ratio 10/1. 10 = deliver high/low packets at ratio 5/1. 11 = deliver high/low packets at ratio 2/1.	R/W	00
1	Enable “Tag” Mask	1, the last 5 digits in the VID field are used as a mask to determine which port(s) the packet should be forwarded to. 0, no tag masks.	R/W	0
0	Sniff Mode Select	1, will do Rx AND Tx sniff (both source port and destination port need to match). 0, will do Rx OR Tx sniff (Either source port or destination port needs to match). This is the mode used to implement Rx only sniff.	R/W	0
Register 6 (0x06): Global Control 4				
7	Switch MII Back Pressure Enable	1, enable half-duplex back pressure on switch MII interface. 0, disable back pressure on switch MII interface.	R/W	0
6	Switch MII Half-Duplex Mode	1, enable MII interface half-duplex mode. 0, enable MII interface full-duplex mode.	R/W	Pin SMRXD2 strap option. Pull-down (0): Full-duplex mode. Pull-up (1): Half-duplex mode. Note: SMRXD2 has internal pull-down.

Address	Name	Description	Mode	Default[1]
5	Switch MII Flow Control Enable	1, enable full-duplex flow control on switch MII interface. 0, disable full-duplex flow control on switch MII interface.	R/W	Pin SMRXD3 strap option. Pull-down (0): disable flow control. Pull-up(1): enable flow control. Note: SMRXD3 has internal pull-down.
4	Switch MII 10BT	1, the switch interface is in 10Mbps mode. 0, the switch interface is in 100Mbps mode.	R/W	Pin SMRXD1 strap option. Pull-down (0): Enable 100Mbps. Pull-up (1): Enable 10Mpbs. Note: SMRXD1 has internal pull-down.
3	Null VID Replacement	1, will replace null VID with port VID (12 bits). 0, no replacement for null VID.	R/W	0
2-0	Broadcast Storm Protection Rate Bit [10:8]	This along with the next register determines how many “64 byte blocks” of packet data allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%.	R/W	000
Register 7 (0x07): Global Control 5				
7-0	Broadcast Storm Protection Rate Bit [7:0]	This along with the previous register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%.	R/W	0x4A[1]

Note:

1. 148,800 frames/sec × 50ms/interval × 1% = 74 frames/interval (approximately) = 0x4A.

Register 8 (0x08): Global Control 6				
7-0	Factory Testing	Reserved.	R/W	0x24
Register 9 (0x09): Global Control 7				
7-0	Factory Testing	Reserved.	R/W	0x28
Register 10 (0x0A): Global Control 8				
7-0	Factory Testing	Reserved.	R/W	0x24
Register 11 (0x0B): Global Control 9				
7-4	Reserved	N/A		0
3	PHY Power Save	0 = disable PHY power save mode. 1 = enable PHY power save mode.	R/W	0
2	Factory Setting	Reserved.	R/W	0
1	LED Mode	0 = led mode 0. 1 = led mode 1. (see LED mode table below)	R/W	Pin SMRXD0 strap option. Pull-down(0): Enabled led mode 0. Pull-up(1): Enabled led mode 1. Note: SMRXD0 has internal pull-down 0.
0	Special TPID Mode	Used for direct mode forwarding from port 5. See “Spanning Tree” functional description.	R/W	0

	Mode 0	Mode 1
LEDX_2	Lnk/Act	100Lnk/Act
LEDX_1	Fulld/Col	10Lnk/Act
LEDX_0	Speed	Fulld

Port Registers

The following registers are used to enable features that are assigned on a per port basis. The register bit assignments are the same for all ports, but the address for each port is different, as indicated.

Register 16 (0x10): Port 1 Control 0
Register 32 (0x20): Port 2 Control 0
Register 48 (0x30): Port 3 Control 0
Register 64 (0x40): Port 4 Control 0
Register 80 (0x50): Port 5 Control 0

Address	Name	Description	Mode	Default
7	Broadcast Storm Protection Enable	1, enable broadcast storm protection for ingress packets on the port. 0, disable broadcast storm protection.	R/W	0
6	DiffServ Priority Classification Enable	1, enable DiffServ priority classification for ingress packets on port. 0, disable DiffServ function.	R/W	0
5	802.1p Priority Classification Enable	1, enable 802.1p priority classification for ingress packets on port. 0, disable 802.1p.	R/W	0
4	Port-Based Priority Classification Enable	1, ingress packets on the port will be classified as high priority if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 0, ingress packets on port will be classified as low priority if “DiffServ” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.	R/W	0
3	Reserved	Reserved.	R/W	0
2	Tag Insertion	1, when packets are output on the port, the switch will add 802.1q tags to packets without 802.1q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID.” 0, disable tag insertion.	R/W	0
1	Tag Removal	1, when packets are output on the port, the switch will remove 802.1q tags from packets with 802.1q tags when received. The switch will not modify packets received without tags. 0, disable tag removal.	R/W	0
0	Priority Enable	1, the port output queue is split into high and low priority queues. 0, single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.	R/W	0

Register 17 (0x11): Port 1 Control 1
Register 33 (0x21): Port 2 Control 1
Register 49 (0x31): Port 3 Control 1
Register 65 (0x41): Port 4 Control 1
Register 81 (0x51): Port 5 Control 1

Address	Name	Description	Mode	Default
7	Sniffer Port	1, port is designated as sniffer port and will transmit packets that are monitored. 0, Port is a normal port.	R/W	0
6	Receive Sniff	1, all the packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port.” 0, no receive monitoring.	R/W	0

Address	Name	Description	Mode	Default
5	Transmit Sniff	1, All the packets transmitted on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port." 0, no transmit monitoring.	R/W	0
4-0	Port VLAN Membership	Define the port's "Port VLAN membership." Bit 4 stands for port 5, bit 3 for port 4...bit 0 for port 1. The port can only communicate within the membership. A '1' includes a port in the membership, a '0' excludes a port from membership.	R/W	0x1f

Register 18 (0x12): Port 1 Control 2
Register 34 (0x22): Port 2 Control 2
Register 50 (0x32): Port 3 Control 2
Register 66 (0x42): Port 4 Control 2
Register 82 (0x52): Port 5 Control 2

Address	Name	Description	Mode	Default
7	Reserved	Reserved.		0x0
6	Ingress VLAN Filtering.	1, the switch will discard packets whose VID port membership in VLAN table bit[20:16] does not include the ingress port. 0, no ingress VLAN filtering.	R/W	0
5	Discard Non-PVID Packets.	1, the switch will discard packets whose VID does not match ingress port default VID. 0, no packets will be discarded.	R/W	0
4	Force Flow Control	1, will always enable Rx and Tx flow control on the port, regardless of AN result. 0, the flow control is enabled based on AN result. Note: Setting a port for both half-duplex and forced flow control is an illegal configuration. For half-duplex enable back pressure.	R/W	0 For port 4 only, there is a special configuration pin to set the default, Pin PCOL strap option. Pull-down (0): No Force flow control. Pull-up (1): Force flow control. Note: PCOL has internal pull-down.
3	Back Pressure Enable	1, enable port's half-duplex back pressure. 0, disable port's half-duplex back pressure.	R/W	Pin PMRXD2 strap option. Pull-down (0): disable back pressure. Pull-up (1): enable back pressure. Note: PMRXD2 has internal pull-down.
2	Transmit Enable	1, enable packet transmission on the port. 0, disable packet transmission on the port.	R/W	1
1	Receive Enable	1, enable packet reception on the port. 0, disable packet reception on the port.	R/W	1
0	Learning Disable	1, disable switch address learning capability. 0, enable switch address learning.	R/W	0

Note:
Bits 2-0 are used for spanning tree support. See "Spanning Tree Support" section.

Register 19 (0x13): Port 1 Control 3
Register 35 (0x23): Port 2 Control 3
Register 51 (0x33): Port 3 Control 3
Register 67 (0x43): Port 4 Control 3
Register 83 (0x53): Port 5 Control 3

Address	Name	Description	Mode	Default
7-0	Default Tag [15:8]	Port's default tag, containing: 7-5: user priority bits 4: CFI bit 3-0 : VID[11:8]	R/W	0

Register 20 (0x14): Port 1 Control 4
Register 36 (0x24): Port 2 Control 4
Register 52 (0x34): Port 3 Control 4
Register 68 (0x44): Port 4 Control 4
Register 84 (0x54): Port 5 Control 4

Address	Name	Description	Mode	Default
7-0	Default Tag [7:0]	Default port 1's tag, containing: 7-0: VID[7:0]	R/W	1

Note:
Registers 19 and 20 (and those corresponding to other ports) serve two purposes: (1) associated with the ingress untagged packets, and used for egress tagging; (2) default VID for the ingress untagged or null-VID-tagged packets, and used for address look-up.

Register 21 (0x15): Port 1 Control 5
Register 37 (0x25): Port 2 Control 5
Register 53 (0x35): Port 3 Control 5
Register 69 (0x45): Port 4 Control 5
Register 85 (0x55): Port 5 Control 5

Address	Name	Description	Mode	Default
7-0	Transmit High Priority Rate Control [7:0]	This along with port control 7, bits [3:0] form a 12-bit field to determine how many "32Kbps" high priority blocks can be transmitted (in a unit of 4K bytes in a one second period).	R/W	0

Register 22 (0x16): Port 1 Control 6
Register 38 (0x26): Port 2 Control 6
Register 54 (0x36): Port 3 Control 6
Register 70 (0x46): Port 4 Control 6
Register 86 (0x56): Port 5 Control 6

Address	Name	Description	Mode	Default
7-0	Transmit Low Priority Rate Control [7:0]	This along with port control 7, bits [7:4] form a 12-bit field to determine how many "32Kbps" low priority blocks can be transmitted (in a unit of 4K bytes in a one second period).	R/W	0

Register 23 (0x17): Port 1 Control 7
Register 39 (0x27): Port 2 Control 7
Register 55 (0x37): Port 3 Control 7
Register 71 (0x47): Port 4 Control 7
Register 87 (0x57): Port 5 Control 7

Address	Name	Description	Mode	Default
7-4	Transmit Low Priority Rate Control [11:8]	This along with port control 6, bits [7:0] form a 12-bit field to determine how many "32Kbps" low priority blocks can be transmitted (in a unit of 4K bytes in a one second period).	R/W	0
3-0	Transmit High Priority Rate Control [11:8]	This along with port control 5, bits [7:0] form a 12-bit field to determine how many "32Kbps" high priority blocks can be transmitted (in unit of 4K bytes in a one second period).	R/W	0

Register 24 (0x18): Port 1 Control 8
Register 40 (0x28): Port 2 Control 8
Register 56 (0x38): Port 3 Control 8
Register 72 (0x48): Port 4 Control 8
Register 88 (0x58): Port 5 Control 8

Address	Name	Description	Mode	Default
7-0	Receive High Priority Rate Control [7:0]	This along with port control 10, bits [3:0] form a 12-bit field to determine how many “32Kbps” high priority blocks can be received (in a unit of 4K bytes in a one second period).	R/W	0

Register 25 (0x19): Port 1 Control 9
Register 41 (0x29): Port 2 Control 9
Register 57 (0x39): Port 3 Control 9
Register 73 (0x49): Port 4 Control 9
Register 89 (0x59): Port 5 Control 9

Address	Name	Description	Mode	Default
7-0	Receive Low Priority Rate Control [7:0]	This along with port control 10, bits [7:4] form a 12-bit field to determine how many “32Kbps” low priority blocks can be received (in a unit of 4K bytes in a one second period).	R/W	0

Register 26 (0x1A): Port 1 Control 10
Register 42 (0x2A): Port 2 Control 10
Register 58 (0x3A): Port 3 Control 10
Register 74 (0x4A): Port 4 Control 10
Register 90 (0x5A): Port 5 Control 10

Address	Name	Description	Mode	Default
7-4	Receive Low Priority Rate Control [11:8]	This along with port control 9, bits [7:0] form a 12-bit field to determine how many “32Kbps” low priority blocks can be received (in a unit of 4K bytes in a one second period).	R/W	0
3-0	Receive High Priority Rate Control [11:8]	This along with port control 8, bits [7:0] form a 12-bit field to determine how many “32Kbps” high priority blocks can be received (in a unit of 4K bytes in a one second period).	R/W	0

Register 27 (0x1B): Port 1 Control 11
Register 43 (0x2B): Port 2 Control 11
Register 59 (0x3B): Port 3 Control 11
Register 75 (0x4B): Port 4 Control 11
Register 91 (0x5B): Port 5 Control 11

Address	Name	Description	Mode	Default
7	Receive Differential Priority Rate Control	1, If bit 6 is also ‘1’ this will enable receive rate control for this port on low priority packets at the low priority rate. If bit 5 is also ‘1’, this will enable receive rate control on high priority packets at the high priority rate. 0, receive rate control will be based on the low priority rate for all packets on this port.	R/W	0
6	Low Priority Receive Rate Control Enable	1, enable port’s low priority receive rate control feature. 0, disable port’s low priority receive rate control.	R/W	0
5	High Priority Receive Rate Control Enable	1, If bit 7 is also ‘1’ this will enable the port’s high priority receive rate control feature. If bit 7 is a ‘0’ and bit 6 is a ‘1’, all receive packets on this port will be rate controlled at the low priority rate. 0, disable port’s high priority receive rate control feature.	R/W	0
4	Low Priority Receive Rate Flow Control Enable	1, flow control may be asserted if the port’s low priority receive rate is exceeded. 0, flow control is not asserted if the port’s low priority receive rate is exceeded.	R/W	0

Address	Name	Description	Mode	Default
3	High Priority Receive Rate Flow Control Enable	1, flow control may be asserted if the port's high priority receive rate is exceeded (to use this, differential receive rate control must be on). 0, flow control is not asserted if the port's high priority receive rate is exceeded.	R/W	0
2	Transmit Differential Priority Rate Control	1, will do transmit rate control on both high and low priority packets based on the rate counters defined by the high and low priority packets respectively. 0, will do transmit rate control on any packets. The rate counters defined in low priority will be used.	R/W	0
1	Low Priority Transmit Rate Control Enable	1, enable the port's low priority transmit rate control feature. 0, disable the port's low priority transmit rate control feature.	R/W	0
0	High Priority Transmit Rate Control Enable	1, enable the port's high priority transmit rate control feature 0, disable the port's high priority transmit rate control feature.	R/W	0

Register 28 (0x1C): Port 1 Control 12
Register 44 (0x2C): Port 2 Control 12
Register 60 (0x3C): Port 3 Control 12
Register 76 (0x4C): Port 4 Control 12
Register 92 (0x5C): Port 5 Control 12

Address	Name	Description	Mode	Default
7	Disable Auto-Negotiation	1, disable auto-negotiation, speed and duplex are decided by bit 6 and 5 of the same register. 0, auto-negotiation is on.	R/W	0
6	Forced Speed	1, forced 100BT if AN is disabled (bit 7). 0, forced 10BT if AN is disabled (bit 7).	R/W	1
5	Forced Duplex	1, forced full-duplex if (1) AN is disabled or (2) AN is enabled but failed. 0, forced half-duplex if (1) AN is disabled or (2) AN is enabled but failed.	R/W	0 For port 4 only, there is a special configure pin to set the default, Pin PCRS strap option. Pull-down (0): Force half-duplex. Pull-up (1): Force full-duplex. Note: PCRS has internal pull down.
4	Advertised Flow Control Capability	1, advertise flow control capability. 0, suppress flow control capability from transmission to link partner.	R/W	1
3	Advertised 100BT Full-Duplex Capability	1, advertise 100BT full-duplex capability. 0, suppress 100BT full-duplex capability from transmission to link partner.	R/W	1
2	Advertised 100BT Half-Duplex Capability	1, advertise 100BT half-duplex capability. 0, suppress 100BT half-duplex capability from transmission to link partner.	R/W	1
1	Advertised 10BT Full-Duplex Capability	1, advertise 10BT full-duplex capability. 0, suppress 10BT full-duplex capability from transmission to link partner.	R/W	0

Address	Name	Description	Mode	Default
0	Advertised 10BT Half-Duplex Capability	1, advertise 10BT half-duplex capability. 0, suppress 10BT half-duplex capability from transmission to link partner.	R/W	1

Note:
Port Control 12 and 13, and Port Status 0 contents can be accessed by MIIM (MDC/MDIO) interface via the standard MIIM register definition.

Register 29 (0x1D): Port 1 Control 13
Register 45 (0x2D): Port 2 Control 13
Register 61 (0x3D): Port 3 Control 13
Register 77 (0x4D): Port 4 Control 13
Register 93 (0x5D): Port 5 Control 13

Address	Name	Description	Mode	Default
7	LED Off	1, Turn off all port's LEDs (LEDx_2, LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one. 0, normal operation.	R/W	0
6	Txids	1, disable port's transmitter. 0, normal operation.	R/W	0
5	Restart AN	1, restart auto-negotiation. 0, normal operation.	R/W	0
4	Disable Far End Fault	1, disable far end fault detection and pattern transmission. 0, enable far end fault detection and pattern transmission.	R/W	0
3	Power Down	1, power down. 0, normal operation.	R/W	0
2	Disable Auto MDI/MDI-X	1, disable auto MDI/MDI-X function. 0, enable auto MDI/MDI-X function.	R/W	0
1	Forced MDI	1, If auto MDI/MDI-X is disabled, force PHY into MDI mode. 0, Do not force PHY into MDI mode.	R/W	0
0	MAC Loopback	1, Perform MAC loopback. 0, normal operation.	R/W	0

Register 30 (0x1E): Port 1 Status 0
Register 46 (0x2E): Port 2 Status 0
Register 62 (0x3E): Port 3 Status 0
Register 78 (0x4E): Port 4 Status 0
Register 94 (0x5E): Port 5 Status 0

Address	Name	Description	Mode	Default
7	MDI-X Status	1, MDI. 0, MDI-X.	RO	0
6	AN Done	1, AN done. 0, AN not done.	RO	0
5	Link Good	1, link good. 0, link not good.	RO	0
4	Partner Flow Control Capability	1, link partner flow control capable. 0, link partner not flow control capable.	RO	0
3	Partner 100BT Full-Duplex Capability	1, link partner 100BT full-duplex capable. 0, link partner not 100BT full-duplex capable.	RO	0
2	Partner 100BT Half-Duplex Capability	1, link partner 100BT half-duplex capable. 0, link partner not 100BT half-duplex capable.	RO	0
1	Partner 10BT Full-Duplex Capability	1, link partner 10BT full-duplex capable. 0, link partner not 10BT full-duplex capable.	RO	0
0	Partner 10BT Half-Duplex Capability	1, link partner 10BT half-duplex capable. 0, link partner not 10BT half-duplex capable.	RO	0

Register 31 (0x1F): Port 1 Control 14
Register 47 (0x2F): Port 2 Control 14
Register 63 (0x3F): Port 3 Control 14
Register 79 (0x4F): Port 4 Control 14
Register 95 (0x5F): Port 5 Control 14

Address	Name	Description	Mode	Default
7	PHY Loopback	1, perform PHY loopback, i.e. loopback MAC's Tx back to Rx. 0, normal operation.	R/W	0
6	Remote Loopback	1, perform remote loopback, i.e. loopback PHY's Rx back to Tx. 0, normal operation.	R/W	0
5	PHY Isolate	1, electrical isolation of PHY from MII and Tx+/Tx-. 0, normal operation.	R/W	0
4	Soft Reset	1, PHY soft reset. 0, normal operation.	R/W	0
3	Force Link	1, Force link in the PHY. 0, normal operation.	R/W	0
2-1	Reserved	N/A	RO	0
0	Far End Fault	1, Far end fault status detected. 0, no far end fault status detected.	RO	0

Advanced Control Registers

The IPv4 TOS priority control registers implement a fully decoded 64 bit differentiated services code point (DSCP) register used to determine priority from the 6 bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high; if the register bit is a 0, the priority is low.

Address	Name	Description	Mode	Default
Register 96 (0x60): TOS Priority Control Register 0				
7-0	DSCP[63:56]		R/W	00000000
Register 97 (0x61): TOS Priority Control Register 1				
7-0	DSCP[55:48]		R/W	00000000
Register 98 (0x62): TOS Priority Control Register 2				
7-0	DSCP[47:40]		R/W	00000000
Register 99 (0x63): TOS Priority Control Register 3				
7-0	DSCP[39:32]		R/W	00000000
Register 100 (0x64): TOS Priority Control Register 4				
7-0	DSCP[31:24]		R/W	00000000
Register 101 (0x65): TOS Priority Control Register 5				
7-0	DSCP[23:16]		R/W	00000000
Register 102 (0x66): TOS Priority Control Register 6				
7-0	DSCP[15:8]		R/W	00000000
Register 103 (0x67): TOS Priority Control Register 7				
7-0	DSCP[7:0]		R/W	00000000

Registers 104 to 109 define the switching engine's MAC address. This 48-bit address is used as the source address in MAC pause control frames.

Register 104 (0x68): MAC Address Register 0				
7-0	MACA[47:40]		R/W	0x00
Register 105 (0x69): MAC Address Register 1				
7-0	MACA[39:32]		R/W	0x10

Address	Name	Description	Mode	Default
Register 106 (0x6A): MAC Address Register 2				
7-0	MACA[31:24]		R/W	0xA1
Register 107 (0x6B): MAC Address Register 3				
7-0	MACA[23:16]		R/W	0xff
Register 108 (0x6C): MAC Address Register 4				
7-0	MACA[15:8]		R/W	0xff
Register 109 (0X6D): MAC Address Register 5				
7-0	MACA[7:0]		R/W	0xff

Use registers 110 and 111 to read or write data to the static MAC address table, VLAN table, dynamic address table, or the MIB counters.

Address	Name	Description	Mode	Default
Register 110 (0x6E): Indirect Access Control 0				
7-5	Reserved	Reserved.	R/W	000
4	Read High Write Low	1, read cycle. 0, write cycle.	R/W	0
3-2	Table Select	00 = static mac address table selected. 01 = VLAN table selected. 10 = dynamic address table selected. 11 = MIB counter selected.	R/W	0
1-0	Indirect Address High	Bit 9-8 of indirect address.	R/W	00
Register 111 (0x6F): Indirect Access Control 1				
7-0	Indirect Address Low	Bit 7-0 of indirect address.	R/W	00000000

Note:
Write to Register 111 will actually trigger a command. Read or write access will be decided by bit 4 of Register 110.

Address	Name	Description	Mode	Default
Register 112 (0x70): Indirect Data Register 8				
68-64	Indirect Data	Bit 68-64 of indirect data.	R/W	00000
Register 113 (0x71): Indirect Data Register 7				
63-56	Indirect Data	Bit 63-56 of indirect data.	R/W	00000000
Register 114 (0x72): Indirect Data Register 6				
55-48	Indirect Data	Bit 55-48 of indirect data.	R/W	00000000
Register 115 (0x73): Indirect Data Register 5				
47-40	Indirect Data	Bit 47-40 of indirect data.	R/W	00000000
Register 116 (0x74): Indirect Data Register 4				
39-32	Indirect Data	Bit 39-32 of indirect data.	R/W	00000000
Register 117 (0x75): Indirect Data Register 3				
31-24	Indirect Data	Bit of 31-24 of indirect data	R/W	00000000
Register 118 (0x76): Indirect Data Register 2				
23-16	Indirect Data	Bit 23-16 of indirect data.	R/W	00000000
Register 119 (0x77): Indirect Data Register 1				
15-8	Indirect Data	Bit 15-8 of indirect data.	R/W	00000000
Register 120 (0x78): Indirect Data Register 0				
7-0	Indirect Data	Bit 7-0 of indirect data.	R/W	00000000

Do not write or read to/from Register isters 121 to 127. Doing so may prevent proper operation. Micrel internal testing only.

Address	Name	Description	Mode	Default
Register 121 (0x79): Digital Testing Status 0				
7-0	Factory Testing	Reserved. Qm_split status	RO	0x0
Register 122 (0x7A): Digital Testing Status 1				
7-0	Factory Testing	Reserved. Dbg[7:0]	RO	0x0
Register 123 (0x7B): Digital Testing Control 0				
7-0	Factory Testing	Reserved. Dbg[12:8]	R/W	0x0
Register 124 (0x7C): Digital Testing Control 1				
7-0	Factory Testing	Reserved.	R/W	0x0
Register 125 (0x7D): Analog Testing Control 0				
7-0	Factory Testing	Reserved.	R/W	0x0
Register 126 (0x7E): Analog Testing Control 1				
7-0	Factory Testing	Reserved.	R/W	0x0
Register 127 (0x7F): Analog Testing Status				
7-0	Factory Testing	Reserved.	RO	0x0

Static MAC Address

KS8995MA has a static and a dynamic address table. When a DA look-up is requested, both tables will be searched to make a packet forwarding decision. When an SA look-up is requested, only the dynamic table is searched for aging, migration, and learning purposes. The static DA look-up result will have precedence over the dynamic DA look-up result. If there are DA matches in both tables, the result from the static table will be used. The static table can only be accessed and controlled by an external SPI master (usually a processor). The entries in the static table will not be aged out by KS8995MA. An external device does all addition, modification and deletion.

Note:
Register bit assignments are different for static MAC table reads and static MAC table write, as shown in the two tables below.

Address	Name	Description	Mode	Default
Format of Static MAC Table for Reads (8 entries)				
60-57	FID	Filter VLAN ID, representing one of the 16 active VLANs.	RO	0000
56	Use FID	1, use (FID+MAC) to look-up in static table. 0, use MAC only to look-up in static table.	RO	0
55	Reserved	Reserved.	RO	N/A
54	Override	1, override spanning tree “transmit enable = 0” or “receive enable = 0” setting. This bit is used for spanning tree implementation. 0, no override.	RO	0
53	Valid	1, this entry is valid, the look-up result will be used. 0, this entry is not valid.	RO	0
52-48	Forwarding Ports	The 5 bits control the forward ports, example: 00001, forward to port 1 00010, forward to port 2 ..... 10000, forward to port 5 00110, forward to port 2 and port 3 11111, broadcasting (excluding the ingress port)	RO	00000
47-0	MAC Address	48 bit MAC address.	RO	0x0
Format of Static MAC Table for Writes (8 entries)				
59-56	FID	Filter VLAN ID, representing one of the 16 active VLANs.	W	0000
55	Use FID	1, use (FID+MAC) to look-up in static table. 0, use MAC only to look-up in static table.	W	0
54	Override	1, override spanning tree “transmit enable = 0” or “receive enable = 0” setting. This bit is used for spanning tree implementation. 0, no override.	W	0
53	Valid	1, this entry is valid, the look-up result will be used. 0, this entry is not valid.	W	0
52-48	Forwarding Ports	The 5 bits control the forward ports, example: 00001, forward to port 1 00010, forward to port 2 ..... 10000, forward to port 5 00110, forward to port 2 and port 3 11111, broadcasting (excluding the ingress port)	W	00000
47-0	MAC Address	48-bit MAC address.	W	0x0

Table 12. Static MAC Address Table

Examples:

(1) Static Address Table Read (read the 2nd entry)

Write to Register 110 with 0x10 (read static table selected)
Write to Register 111 with 0x1 (trigger the read operation)
Then
Read Register 113 (60-56)
Read Register 114 (55-48)
Read Register 115 (47-40)
Read Register 116 (39-32)
Read Register 117 (31-24)
Read Register 118 (23-16)
Read Register 119 (15-8)
Read Register 120 (7-0)

(2) Static Address Table Write (write the 8th entry)

Write Register 113 (59-56)
Write Register 114 (55-48)
Write Register 115 (47-40)
Write Register 116 (39-32)
Write Register 117 (31-24)
Write Register 118 (23-16)
Write Register 119 (15-8)
Write Register 120 (7-0)
Write to Register 110 with 0x00 (write static table selected)
Write to Register 111 with 0x7 (trigger the write operation)

VLAN Address

The VLAN table is used for VLAN table look-up. If 802.1q VLAN mode is enabled (Register 5 bit 7 =1), this table is used to retrieve VLAN information that is associated with the ingress packet. The information includes FID (filter ID), VID (VLAN ID), and VLAN membership described below:

Address	Name	Description	Mode	Default
Format of Static VLAN Table (16 entries)				
21	Valid	1, the entry is valid. 0, entry is invalid.	R/W	1
20-16	Membership	Specify which ports are members of the VLAN. If a DA look-up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. E.g., 11001 means port 5, 4, and 1 are in this VLAN.	R/W	11111
15-12	FID	Filter ID. KS8995MA supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1q VLAN is enabled, the look-up will be based on FID+DA and FID+SA.	R/W	0
11-0	VID	IEEE 802.1q 12 bit VLAN ID.	R/W	1

Table 13. VLAN Table

If 802.1q VLAN mode is enabled, KS8995MA assigns a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, the VID in the tag is used. The look-up process starts from the VLAN table look-up. If the VID is not valid, the packet is dropped and no address learning occurs. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look-up determines the forwarding ports. If FID+DA fails, the packet is broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA is learned.

Examples:

(1) VLAN Table Read (read the 3rd entry)

Write to Register 110 with 0x14 (read VLAN table selected)
Write to Register 111 with 0x2 (trigger the read operation)
Then
Read Register 118 (VLAN table bits 21-16)
Read Register 119 (VLAN table bits 15-8)
Read Register 120 (VLAN table bits 7-0)

(2) VLAN Table Write (write the 7th entry)

Write to Register 118 (VLAN table bits 21-16)
Write to Register 119 (VLAN table bits 15-8)
Write to Register 120 (VLAN table bits 7-0)
Write to Register 110 with 0x04 (write static table selected)
Write to Register 111 with 0x6 (trigger the write operation)

Dynamic MAC Address

This table is read only. The contents are maintained by the KS8995MA only.

Address	Name	Description	Mode	Default
Format of Dynamic MAC Address Table (1K entries)				
68	MAC Empty	1, there is no valid entry in the table. 0, there are valid entries in the table.	RO	1
67-58	No of Valid Entries	Indicates how many valid entries in the table. 0x3ff means 1K entries 0x1 means 2 entries 0x0 and bit 68 = 0: means 1 entry 0x0 and bit 68 = 1: means 0 entry	RO	0
57-56	Time Stamp	2-bit counters for internal aging	RO	
55	Data Ready	1, The entry is not ready, retry until this bit is set to 0. 0, The entry is ready.	RO	
54-52	Source Port	The source port where FID+MAC is learned. 000 port 1 001 port 2 010 port 3 011 port 4 100 port 5	RO	0x0
51-48	FID	Filter ID.	RO	0x0
47-0	MAC Address	48-bit MAC address.	RO	0x0

Table 14. Dynamic MAC Address Table

Examples:

(1) Dynamic MAC Address Table Read (read the 1st entry), and retrieve the MAC table size

Write to Register 110 with 0x18 (read dynamic table selected)

Write to Register 111 with 0x0 (trigger the read operation)

Then

Read Register 112 (68-64)

Read Register 113 (63-56); // the above two registers show # of entries

Read Register 114 (55-48) // if bit 55 is 1, restart (reread) from this register

Read Register 115 (47-40)

Read Register 116 (39-32)

Read Register 117 (31-24)

Read Register 118 (23-16)

Read Register 119 (15-8)

Read Register 120 (7-0)

(2) Dynamic MAC Address Table Read (read the 257th entry), without retrieving # of entries information

Write to Register 110 with 0x19 (read dynamic table selected)

Write to Register 111 with 0x1 (trigger the read operation)

Then

Read Register 114 (55-48) // if bit 55 is 1, restart (reread) from this register ister

Read Register 115 (47-40)

Read Register 116 (39-32)

Read Register 117 (31-24)

Read Register 118 (23-16)

Read Register 119 (15-8)

Read Register 120 (7-0)

MIB Counters

The MIB counters are provided on per port basis. The indirect memory is as below:

For port 1

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets.
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets.
0x2	RxUndersizePkt	Rx undersize packets w/good CRC.
0x3	RxFragments	Rx fragment packets w/bad CRC, symbol errors or alignment errors.
0x4	RxOversize	Rx oversize packets w/good CRC (max: 1536 or 1522 bytes).
0x5	RxJabbers	Rx packets longer than 1522B w/either CRC errors, alignment errors, or symbol errors (depends on max packet size setting).
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCerror	Rx packets within (64,1522) bytes w/an integral number of bytes and a bad CRC (upper limit depends on max packet size setting).
0x8	RxAlignmentError	Rx packets within (64,1522) bytes w/a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting).
0x9	RxControl8808Pkts	The number of MAC control frames received by a port with 88-08h in EtherType field.
0xA	RxPausePkts	The number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC.
0xB	RxBroadcast	Rx good broadcast packets (not including errored broadcast packets or valid multicast packets).
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, errored multicast packets or valid broadcast packets).
0xD	RxUnicast	Rx good unicast packets.
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length.
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length.
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length.
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length.
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length.
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting).
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets.
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets.
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet.
0x17	TxPausePkts	The number of PAUSE frames transmitted by a port.
0x18	TxBroadcastPkts	Tx good broadcast packets (not including errored broadcast or valid multicast packets).
0x19	TxMulticastPkts	Tx good multicast packets (not including errored multicast packets or valid broadcast packets).
0x1A	TxUnicastPkts	Tx good unicast packets.
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium.
0x1C	TxTotalCollision	Tx total collision, half-duplex only.
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions.
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision.
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision.

Table 15. Port-1 MIB Counter Indirect Memory Offsets

For port 2, the base is 0x20, same offset definition (0x20-0x3f)
For port 3, the base is 0x40, same offset definition (0x40-0x5f)
For port 4, the base is 0x60, same offset definition (0x60-0x7f)
For port 5, the base is 0x80, same offset definition (0x80-0x9f)

Address	Name	Description	Mode	Default
Format of Per Port MIB Counters (16 entries)				
31	Overflow	1, Counter overflow. 0, No Counter overflow.	RO	0
30	Count Valid	1, Counter value is valid. 0, Counter value is not valid.	RO	0
29-0	Counter Values	Counter value.	RO	0

Offset	Counter Name	Description
0x100	Port1 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x101	Port2 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x102	Port3 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x103	Port4 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x104	Port5 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x105	Port1 Rx Drop Packets	Rx packets dropped due to lack of resources.
0x106	Port2 Rx Drop Packets	Rx packets dropped due to lack of resources.
0x107	Port3 Rx Drop Packets	Rx packets dropped due to lack of resources.
0x108	Port4 Rx Drop Packets	Rx packets dropped due to lack of resources.
0x109	Port5 Rx Drop Packets	Rx packets dropped due to lack of resources.

Table 16. All Port Dropped Packet MIB Counters

Address	Name	Description	Mode	Default
Format of All Port Dropped Packet MIB Counters				
30-16	Reserved	Reserved.	N/A	N/A
15-0	Counter Values	Counter value.	RO	0

Note:
All port dropped packet MIB counters do not indicate overflow or validity; therefore the application must keep track of overflow and valid conditions.

Examples:

(1) MIB counter read (read port 1 rx 64 counter)

Write to Register 110 with 0x1c (read MIB counters selected)

Write to Register 111 with 0xe (trigger the read operation)

Then

Read Register 117 (counter value 31-24)
// If bit 31 = 1, there was a counter overflow

// If bit 30 = 0, restart (reread) from this register

Read Register 118 (counter value 23-16)

Read Register 119 (counter value 15-8)

Read Register 120 (counter value 7-0)

(2) MIB counter read (read port 2 rx 64 counter)

Write to Register 110 with 0x1c
(read MIB counter selected)

Write to Register 111 with 0x2e
(trigger the read operation)

Then

Read Register 117 (counter value 31-24)
// If bit 31 = 1, there was a counter overflow

// If bit 30 = 0, restart (reread) from this register

Read Register 118 (counter value 23-16)

Read Register 119 (counter value 15-8)

Read Register 120 (counter value 7-0)

(3) MIB counter read (read port 1 tx drop packets)

Write to Register 110 with 0x1d

Write to Register 111 with 0x00

Then

Read Register 119 (counter value 15-8)

Read Register 120 (counter value 7-0)

Note:
To read out all the counters, the best performance over the SPI bus is (160+3) × 8 × 200 = 260ms, where there are 160 registers, 3 overhead, 8 clocks per access, at 5MHz. In the heaviest condition, the byte counter will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds. The per port MIB counters are designed as “read clear.” A per port MIB counter will be cleared after it is accessed. All port dropped packet MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

MIIM Registers

All the registers defined in this section can be also accessed via the SPI interface. Note: different mapping mechanisms used for MIIM and SPI. The “PHYAD” defined in IEEE is assigned as “0x1” for port 1, “0x2” for port 2, “0x3” for port 3, “0x4” for port 4, and “0x5” for port 5. The “REGAD” supported are 0,1,2,3,4,5.

Address	Name	Description	Mode	Default
Register 0: MII Control				
15	Soft Reset	1, PHY soft reset. 0, Normal operation.	R/W	0
14	Loop Back	1, Loop back mode (loopback at MAC). 0, Normal operation.	R/W	0
13	Force 100	1, 100Mbps. 0, 10Mbps.	R/W	1
12	AN Enable	1, Auto-negotiation enabled. 0, Auto-negotiation disabled.	R/W	1
11	Power Down	1, Power down. 0, Normal operation.	R/W	0
10	PHY Isolate	1, Electrical PHY isolation of PHY from Tx+/Tx-. 0, Normal operation.	R/W	0
9	Restart AN	1, Restart Auto-negotiation. 0, Normal operation.	R/W	0
8	Force Full Duplex	1, Full duplex. 0, Half duplex.	R/W	0
7	Collision Test	Not supported.	RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Force MDI	1, Force MDI. 0, Normal operation.	R/W	0
3	Disable Auto MDI/MDI-X	1, Disable auto MDI/MDI-X. 0, Normal operation.	R/W	0
2	Disable Far End Fault	1, Disable far end fault detection. 0, Normal operation.	R/W	0
1	Disable Transmit	1, Disable transmit. 0, Normal operation.	R/W	0
0	Disable LED	1, Disable LED. 0, Normal operation.	R/W	0

Address	Name	Description	Mode	Default
Register 1: MII Status				
15	T4 Capable	0, Not 100 BASET4 capable.	RO	0
14	100 Full Capable	1, 100BASE-TX full-duplex capable. 0, Not capable of 100BASE-TX full-duplex.	RO	1
13	100 Half Capable	1, 100BASE-TX half-duplex capable. 0, Not 100BASE-TX half-duplex capable.	RO	1
12	10 Full Capable	1, 10BASE-T full-duplex capable. 0, Not 10BASE-T full-duplex capable.	RO	1
11	10 Half Capable	1, 10BASE-T half-duplex capable. 0, 10BASE-T half-duplex capable.	RO	1
10-7	Reserved		RO	0
6	Preamble Suppressed	Not supported.	RO	0
5	AN Complete	1, Auto-negotiation complete. 0, Auto-negotiation not completed.	RO	0
4	Far End Fault	1, Far end fault detected. 0, No far end fault detected.	RO	0
3	AN Capable	1, Auto-negotiation capable. 0, Not auto-negotiation capable.	RO	1
2	Link Status	1, Link is up. 0, Link is down.	RO	0
1	Jabber Test	Not supported.	RO	0
0	Extended Capable	0, Not extended register capable.	RO	0
Register 2: PHYID HIGH				
15-0	Phyid High	High order PHYID bits.	RO	0x0022
Register 3: PHYID LOW				
15-0	Phyid Low	Low order PHYID bits.	RO	0x1450
Register 4: Advertisement Ability				
15	Next Page	Not supported.	RO	0
14	Reserved		RO	0
13	Remote Fault	Not supported.	RO	0
12-11	Reserved		RO	0
10	Pause	1, Advertise pause ability. 0, Do not advertise pause ability.	R/W	1
9	Reserved		R/W	0
8	Adv 100 Full	1, Advertise 100 full-duplex ability. 0, Do not advertise 100 full-duplex ability.	R/W	1
7	Adv 100 Half	1, Advertise 100 half-duplex ability. 0, Do not advertise 100 half-duplex ability.	R/W	1
6	Adv 10 Full	1, Advertise 10 full-duplex ability. 0, Do not advertise 10 full-duplex ability.	R/W	1
5	Adv 10 Half	1, Advertise 10 half-duplex ability. 0, Do not advertise 10 half-duplex ability.	R/W	1
4-0	Selector Field	802.3	RO	00001

Address	Name	Description	Mode	Default
Register 5: Link Partner Ability				
15	Next Page	Not supported.	RO	0
14	LP ACK	Not supported.	RO	0
13	Remote Fault	Not supported.	RO	0
12-11	Reserved		RO	0
10	Pause	Link partner pause capability.	RO	0
9	Reserved		RO	0
8	Adv 100 Full	Link partner 100 full capability.	RO	0
7	Adv 100 Half	Link partner 100 half capability.	RO	0
6	Adv 10 Full	Link partner 10 full capability.	RO	0
5	Adv 10 Half	Link partner 10 half capability.	RO	0
4-0	Reserved		RO	00001

Absolute Maximum Ratings[1]

Supply Voltage
- (V_{DDAR}, V_{DDAP}, V_{DDC}) .... –0.5V to +2.4V
- (V_{DDAT}, V_{DDIO}) .... –0.5V to +4.0V

Input Voltage .... –0.5V to +4.0V

Output Voltage .... –0.5V to +4.0V

Lead Temperature (soldering, 10 sec.) .... 270°C

Storage Temperature (T_S) .... –55°C to +150°C

Operating Ratings[2]

Supply Voltage
- (V_{DDAR}, V_{DDAP}, V_{DDC}) .... +1.7V to +1.9V
- (V_{DDAT}) .... +3.15V to +3.45V or +2.4V to +2.6V
- (V_{DDIO}) .... +3.15V to +3.45V

Ambient Temperature (T_A)
- Commercial .... –0°C to +70°C
- Industrial .... –40°C to +85°C

Package Thermal Resistance[3]
- PQFP (θ_{JA}) No Air Flow .... 59.47°C/W

Electrical Characteristics[4, 5]

Symbol	Parameter	Condition	Min	Typ	Max	Units
100BASE-TX Operation — All Ports 100% Utilization						
I_{DX}	100BASE-TX (Transmitter)	V_{DDAT}		229	250	mA
I_{DDC}	100BASE-TX (Digital Core/PLL + Analog Rx)	V_{DDC}, V_{DDAP}, V_{DDAR}		157	230	mA
I_{DDIO}	100BASE-TX (Digital IO)	V_{DDIO}		17	30	mA
10BASE-TX Operation — All Ports 100% Utilization						
I_{DX}	10BASE-TX (Transmitter)	V_{DDAT}		350	375	mA
I_{DDC}	10BASE-TX (Digital Core + Analog Rx)	V_{DDC}, V_{DDAP}		102	180	mA
I_{DDIO}	10BASE-TX (Digital IO)	V_{DDIO}		6	15	mA
Auto-Negotiation Mode						
I_{DX}	10BASE-TX (Transmitter)	V_{DDAT}		25	40	mA
I_{DDC}	10BASE-TX (Digital Core + Analog Rx)	V_{DDC}, V_{DDAP}		108	180	mA
I_{DDIO}	10BASE-TX (Digital IO)	V_{DDIO}		17	20	mA
TTL Inputs						
V_{IH}	Input High Voltage		+2.0			V
V_{IL}	Input Low Voltage				+0.8	V
I_{IN}	Input Current (Excluding Pull-up/Pull-down)	V_{IN} = GND ~ V_{DDIO}	–10		10	V
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = –8mA	+2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			+0.4	V
$\|I_{OZ}\|$	Output Tri-State Leakage	V_{IN} = GND ~ V_{DDIO}			10	µA
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination on the differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination on the differential output			2	%
t_r, t_t	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns

Notes:
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (ground to V_{DD}).
3. No heat spreader in package.
4. Specification for packaged product only.
5. Measurements were taken within operating ratings.

Symbol	Parameter	Condition	Min	Typ	Max	Units
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
	Duty Cycle Distortion				±0.5	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of I_{SET}			0.5		V
	Output Jitters	Peak-to-peak		0.7	1.4	ns
10BASE-TX Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
10BASE-T Transmit (measured differentially after 1:1 transformer) $V_{DDAT} = 2.5V$						
V_P	Peak Differential Output Voltage	100Ω termination on the differential output		2.3		V
	Jitters Added	100Ω termination on the differential output			16	ns
	Rise/Fall Times			28	30	ns

Timing Diagrams

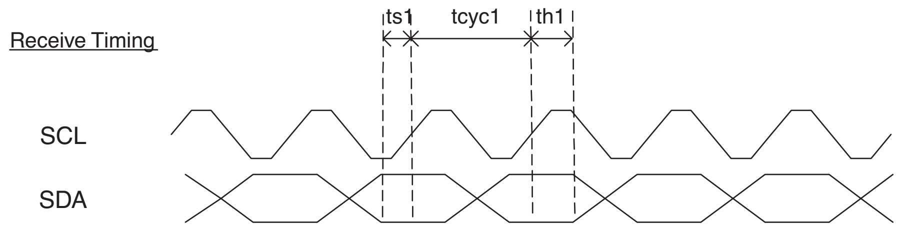


Figure 12. EEPROM Interface Input Receive Timing Diagram

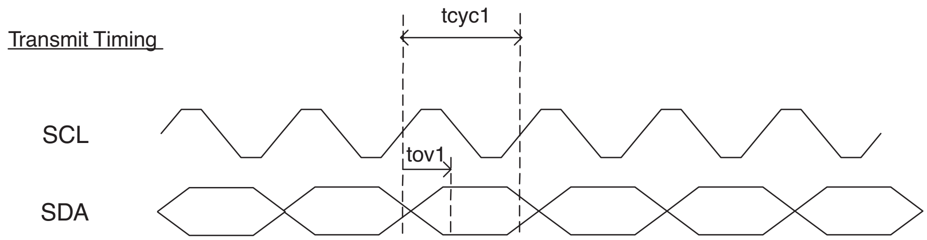


Figure 13. EEPROM Interface Output Transmit Timing Diagram

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC1}	Clock Cycle		16384		ns
t_{S1}	Set-Up Time	20			ns
t_{H1}	Hold Time	20			ns
t_{OV1}	Output Valid	4096	4112	4128	ns

Table 17. EEPROM Timing Parameters

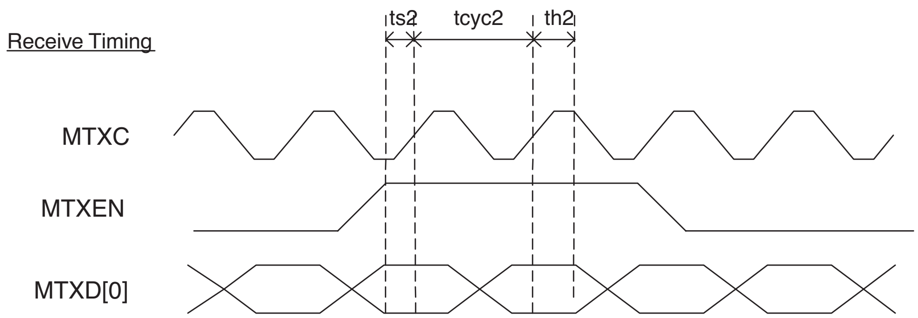


Figure 14. SNI Input Timing

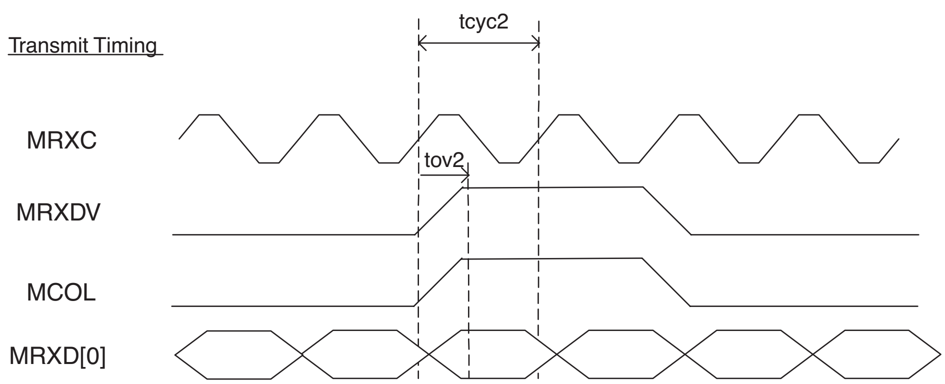


Figure 15. SNI Output Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC2}	Clock Cycle		100		ns
t_{S2}	Set-Up Time	10			ns
t_{H2}	Hold Time	0			ns
t_{O2}	Output Valid	0	3	6	ns

Table 18. SNI Timing Parameters

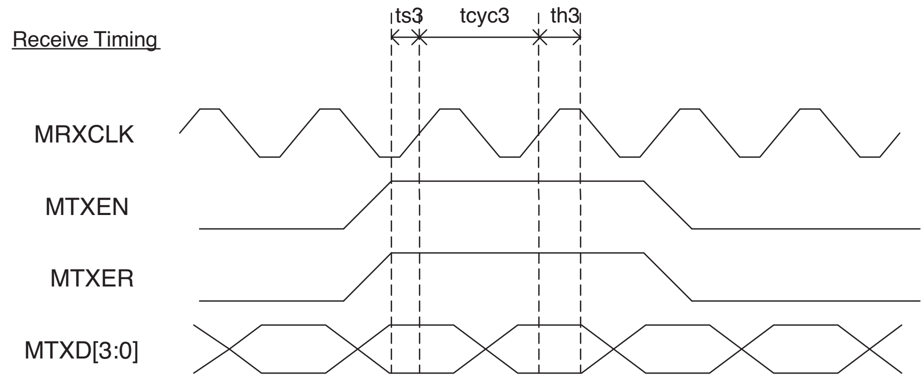


Figure 16. MAC Mode MII Timing – Data Received from MII

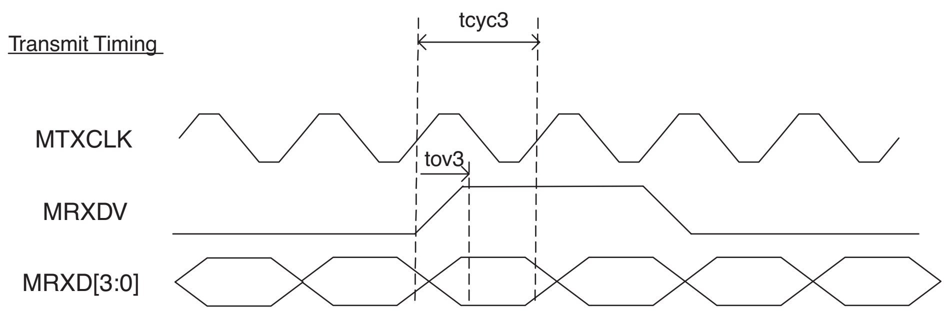


Figure 17. MAC Mode MII Timing – Data Transmitted from MII

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC3}	Clock Cycle (100BASE-T)		40		ns
t_{CYC3}	Clock Cycle (10BASE-T)		400		ns
t_{S3}	Set-Up Time	10			ns
t_{H3}	Hold Time	5			ns
t_{OV3}	Output Valid	7	11	16	ns

Table 19. MAC Mode MII Timing Parameters

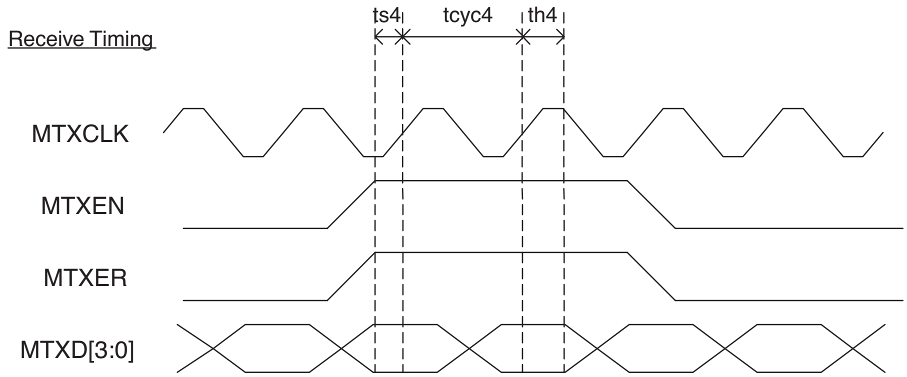


Figure 18. PHY Mode MII Timing – Data Received from MII

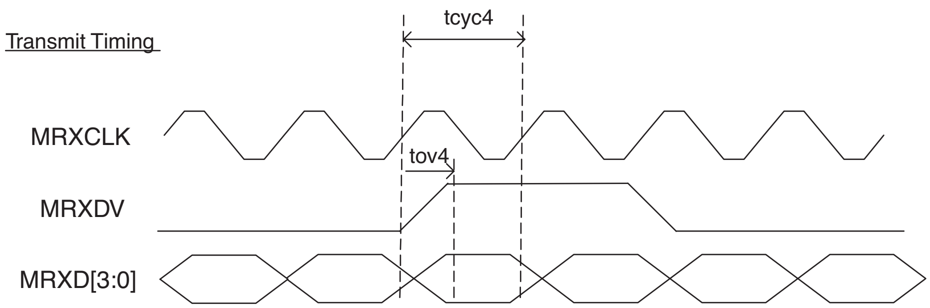


Figure 19. PHY Mode MII Timing – Data Transmitted from MII

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC4}	Clock Cycle (100BASE-T)		40		ns
t_{CYC4}	Clock Cycle (10BASE-T)		400		ns
t_{S4}	Set-Up Time	10			ns
t_{H4}	Hold Time	0			ns
t_{OV4}	Output Valid	18	25	28	ns

Table 20. PHY Mode MII Timing Parameters

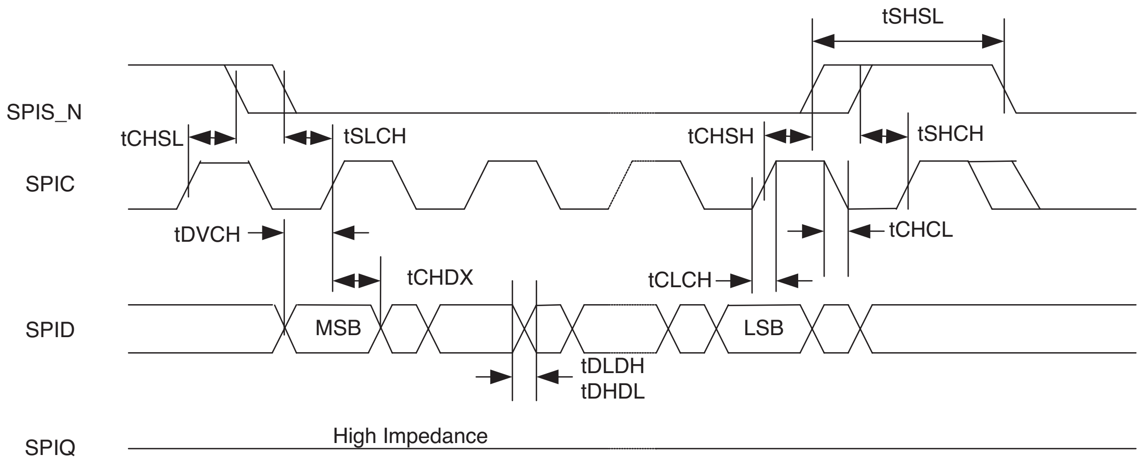


Figure 20. SPI Input Timing

Symbol	Parameter	Min	Typ	Max	Units
f_C	Clock Frequency			5	MHz
t_{CHSL}	SPIS_N Inactive Hold Time	90			ns
t_{SLCH}	SPIS_N Active Set-Up Time	90			ns
t_{CHSH}	SPIS_N Active Hold Time	90			ns
t_{SHCH}	SPIS_N Inactive Set-Up Time	90			ns
t_{SHSL}	SPIS_N Deselect Time	100			ns
t_{DVCH}	Data Input Set-Up Time	20			ns
t_{CHDX}	Data Input Hold Time	30			ns
t_{CLCH}	Clock Rise Time			1	µs
t_{CHCL}	Clock Fall Time			1	µs
t_{DLDH}	Data Input Rise Time			1	µs
t_{DHDL}	Data Input Fall Time			1	µs

Table 21. SPI Input Timing Parameters

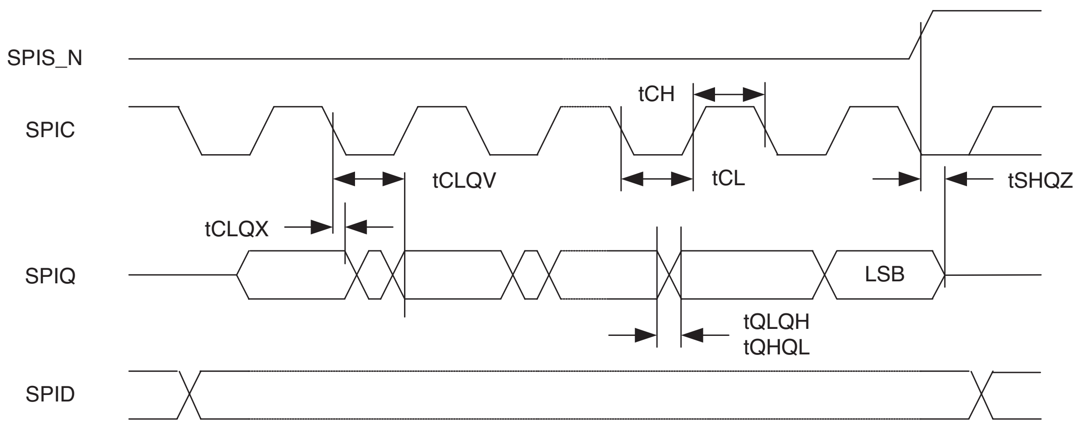


Figure 21. SPI Output Timing

Symbol	Parameter	Min	Typ	Max	Units
f_C	Clock Frequency			5	MHz
t_{CLQX}	SPIQ Hold Time	0		0	ns
t_{CLQV}	Clock Low to SPIQ Valid			60	ns
t_{CH}	Clock High Time	90			ns
t_{CL}	Clock Low Time	90			ns
t_{QLQH}	SPIQ Rise Time			50	ns
t_{QHQL}	SPIQ Fall Time			50	ns
t_{SHQZ}	SPIQ Disable Time			100	ns

Table 22. SPI Output Timing Parameters

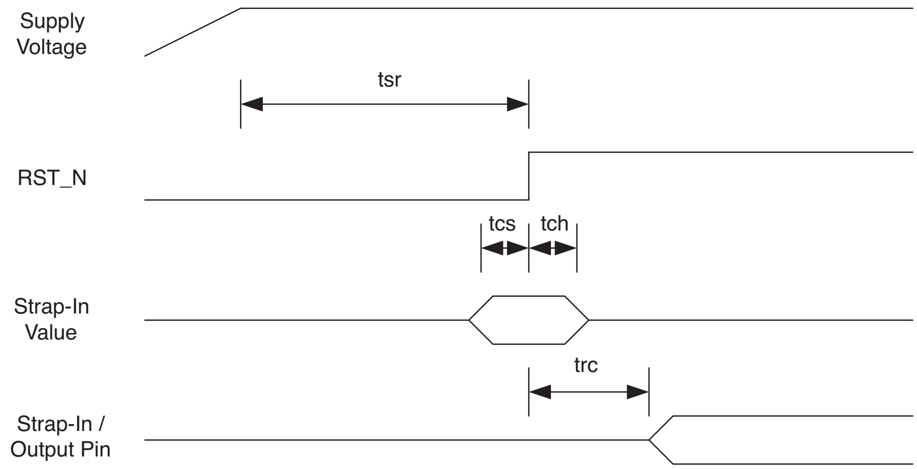


Figure 22. Reset Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{SR}	Stable Supply Voltages to Reset High	10			ms
t_{CS}	Configuration Set-Up Time	50			ns
t_{CH}	Configuration Hold Time	50			ns
t_{RC}	Reset to Strap-In Pin Output	50			ns

Table 23. Reset Timing Parameters

Reset Circuit Diagram

Micrel recommendeds the following discrete reset circuit as shown in Figure 23 when powering up the KS8895MA device. For the application where the reset circuit signal comes from another device (e.g., CPU, FPGA, etc), we recommend the reset circuit as shown in Figure 24.

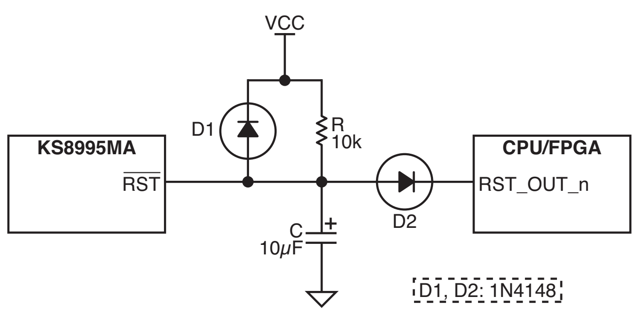


Figure 23. Recommended Reset Circuit.

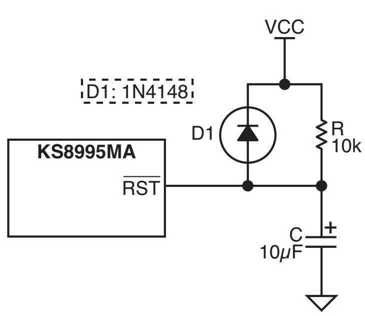


Figure 24. Recommended Circuit for Interfacing with CPU/FPGA Reset

At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the Micrel device. The reset out from CPU/FPGA provides warm reset after power up. It is also recommended to power up the VDD core voltage earlier than VDDIO voltage. At worst case, the both VDD core and VDDIO voltages should come up at the same time.

Selection of Isolation Transformer(1)

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Characteristics Name	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350μH	100mV, 100kHz, 8mA
Leakage Inductance (max.)	0.4μH	1MHz (min.)
Inter-Winding Capacitance (max.)	12pF	
D.C. Resistance (max.)	0.9Ω	
Insertion Loss (max.)	1.0dB	0MHz to 65MHz
Hipot (min.)	1500Vrms	

Note:

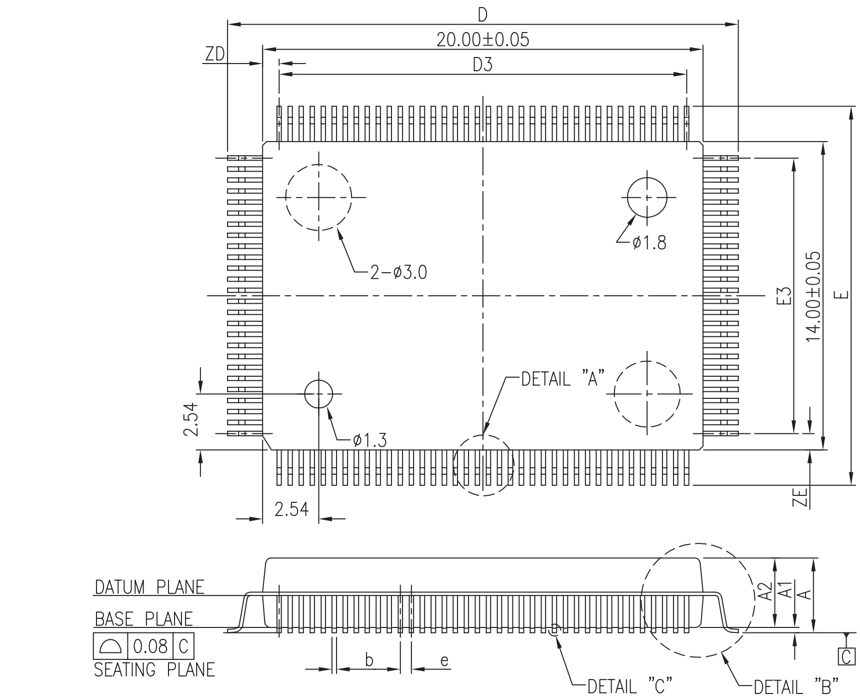
1. The IEEE 802.3u standard for 100BASE-TX assumes a transformer loss of 0.5dB. For the transmit line transformer, insertion loss of up to 1.3dB can be compensated by increasing the line drive current by means of reducing the I_{SET} resistor value.

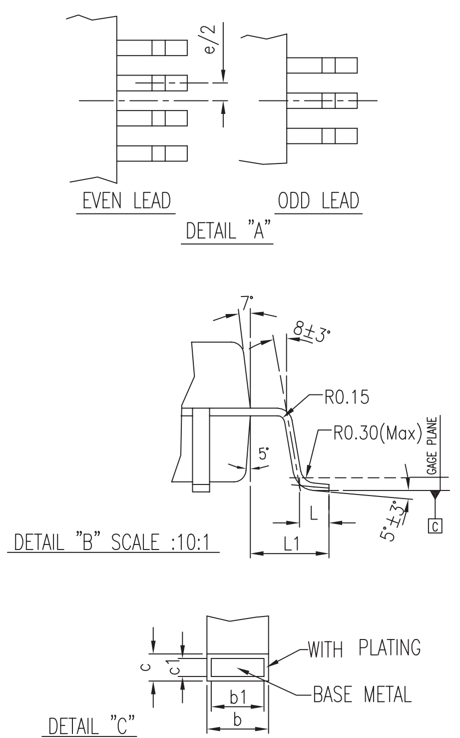
The following transformer vendors provide compatible magnetic parts for Micrel's device:

4-Port Integrated Auto		Number MDI-X	of Port	Single Port	AutoNumber	MDI-X	of Port
Vendor	**Part**			**Vendor**	**Part**		
Pulse	H1164	Yes	4	Pulse	H1102	Yes	1
Bel Fuse	558-5999-Q9	Yes	4	Bel Fuse	S558-5999-U7	Yes	1
YCL	PH406466	Yes	4	YCL	PT163020	Yes	1
Transpower	HB826-2	Yes	4	Transpower	HB726	Yes	1
Delta	LF8731	Yes	4	Delta	LF8505	Yes	1
LanKom	SQ-H48W	Yes	4	LanKom	LF-H41S	Yes	1

Table 24. Qualified Magnetics Vendors

Package Information





DETAIL "A"	ODD	EVEN	EVEN	EVEN
b (MAX.)	0.45	0.40	0.35	0.25
[A] b1 (MAX.)	0.40	0.35	0.30	0.20
c (NOM.)	0.17	0.17	0.17	0.17
[A] c1 (NOM.)	0.15	0.15	0.15	0.15
e (TYP.)	1.00	0.80	0.65	0.50
[A] L1±0.2(REF.)	1.60	1.60	1.60	1.60
L ±0.15	0.80	0.80	0.80	0.80
ZE (TYP.)	1.00	1.00	0.83	0.75
E3 (REF.)	12.00	12.00	12.35	12.50
E ±0.3	17.20	17.20	17.20	17.20
ZD (TYP.)	1.00	0.80	0.58	0.75
D3 (REF.)	18.00	18.40	18.85	18.50
D ±0.3	23.20	23.20	23.20	23.20
A1 (Min.)	0.25	0.25	0.25	0.25
[A] A2 (Nom.)	2.70	2.70	----	----
A (Max.)	3.40	3.40	3.40	3.40
N	64 L	80 L	100 L	128L
JEDEC	MO-112 CA-1	MO-112 CB-1	CC-1	----

128-Pin PQFP (PQ)

MICREL INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com